LEAKAGE POWER REDUCTION TECHNIQUES FOR LOW POWER VLSI DESIGN: A REVIEW PAPER

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ABSTRACT

In this paper covers review of various methods and techniques for reduction of static power dissipation in high performance designs. Static power dissipation becomes serious concern in CMOS technology, because of more percentage of power dissipation is due to leakage power, the percentage of dissipation goes on increasing as scaling in technology. First section contains introduction, second section contains different sources of leakage current and in third section presents review of various effective and simple techniques to reduce leakage power dissipation, and the last section presents conclusion and references.

Keywords: ***Static Power Dissipation, Dynamic Power Dissipation, Leakage Current, Average Power.***

I INTRODUCTION

In today's era of VLSI, a key challenge and critical issue in electronics industry is control and management of power consumption. The advancement in VLSI technology allows integrating a complete system on chip (SoC) providing facility to develop a portable system. The power consumption is the major concerns in VLSI design, the excessive power dissipation in design discourage their use in portable devices. The portable device designing is become more challenging work for VLSI circuit designer as the power consumption become a major concern which leading to reduces the battery life as because of decrease in feature size and corresponding increase in the chip density and operating frequency. The trend in scaling technology increases transistor leakage power expensively, as power consumption or dissipation increases leads to degradation in performance and reduces the design life time. In CMOS design the sources of power consumption mainly due to dynamic power dissipation and leakage power dissipation.

The power consumption can be expressed in equation 1 as below:

$$P_{TOTAL} = P_{DYNAMIC} + P_{STATIC} \quad (1)$$

Where P_{TOTAL} is the total power consumption, $P_{DYNAMIC}$ is the dynamic power consumption due to switching of transistors; P_{STATIC} is the static power consumption.

The dynamic power includes switching power and short circuit power; this cannot be completely eliminated because of computing activity. The static power consumption i.e. the leakage power dissipation has become a

significant portion of total power consumption, it is the power dissipation due to leakage current which flows through a transistor when no transaction occurs and transistor is in steady state, depending on the gate length and thickness of oxide layer. The various techniques reviewed to reduce the leakage power in CMOS VLSI design.

II SOURCES OF LEAKAGE CURRENT

Four main sources of leakage current in MOS transistor as shown in Fig.1 which may leads leakage power dissipation.

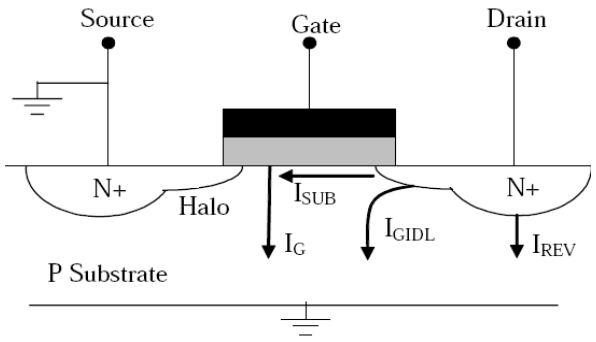

Figure 1. Leakage Current in MOS Transistor

2.1. Junction Leakage (I_{REV})

When the transistor is in OFF state, the junction leakage occurs from the source or drain to the substrate through the reverse biased diodes. The magnitude of the diode's leakage current depends on the area of the drain diffusion and the leakage current density, which is in turn determined by the doping concentration.

2.2. Gate-Induced Drain Leakage (I_{GIDL})

The gate induced drain leakage is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. Transistor scaling has led to increasingly steep *halo* implants, where the substrate doping at the junction interfaces is increased, while the channel doping is low. This is done mainly to control punch-through and drain-induced barrier lowering while having a low impact on the carrier mobility in the channel. The resulting steep doping profile at the drain edge increases band to band tunneling currents there, particularly as VDB is increased. Thinner oxide and higher supply voltage increase GIDL current.

2.3. Gate Direct Tunneling Leakage (I_G)

The gate leakage flows from the gate thru the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4 nm, this kind of current results from the Fowler-Nordheim tunneling of electrons into the conduction

band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses, however, direct tunneling through the silicon oxide layer is the leading effect. Mechanisms for direct tunneling include electron tunneling in the conduction band (ECB), electron tunneling in the valence band (EVB), and hole tunneling in the valence band (HVB), among which ECB is the dominant one. The magnitude of the *gate directs tunneling current* increases exponentially with the gate oxide thickness T_{ox} and supply voltage VDD. In fact, for relatively thin oxide thicknesses, at a V_{GS} of 1V, every 0.2nm reduction in T_{ox} causes a tenfold increase in I_G .

As transistor length and supply voltage are scaled down, gate oxide thickness must also be reduced to maintain effective gate control over the channel region. Unfortunately this results in an exponential increase in the gate leakage due to direct tunneling of electrons through the gate oxide. An effective approach to overcome the gate leakage currents while maintaining excellent gate control is to replace the currently-used silicon dioxide gate insulator with high-K dielectric material such as TiO_2 and Ta_2O_5. Use of the high-k dielectric will allow a less aggressive gate dielectric thickness reduction while maintaining the required gate overdrive at low supply voltages.

2.4. Subthreshold Leakage (I_{SUB})

The sub threshold leakage is the drain-source current of a transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device.

In current CMOS technologies, the subthreshold leakage current, I_{SUB}, is much larger than the other leakage current components. This is mainly because of the relatively low V_T in modern CMOS devices. In long channel devices, the influence of source and drain on the channel depletion layer is negligible. However, as channel lengths are reduced, overlapping source and drain depletion regions cause the depletion region under the inversion layer to increase. The wider depletion region is accompanied by a larger surface potential, which attracts more electrons to the channel. Therefore, a smaller amount of charge on the gate is needed to reach the onset of strong inversion and the threshold voltage decreases. This effect is worsened when there is a larger bias on the drain since the depletion region becomes even wider. More precisely, when a high drain voltage is applied to a short-channel device, it lowers the barrier for electrons between the source and the channel, resulting in further decrease of the threshold voltage. The source then injects carriers into the channel surface, causing an increase in I_{OFF}.

Let I_{OFF} denote the leakage of an OFF transistor (V_{GS}=0V for an NMOS device.), we know that from equation 2. The I_{OFF} can be expressed:

$$\mathbf{I_{OFF}=I_{REV}+I_{GIDL}+I_{SUB}} \qquad \mathbf{(2)}$$

Clearly, I_{REV} and I_{GIDL} are maximized when VDB = VDD. Similarly, for short-channel devices, ISUB increases with VDB because of the DIBL effect. Note the IG is not a component of the OFF current, since the transistor gate must be at a high potential with respect to the source and substrate for this current to flow. Among the three components of I_{OFF}, I_{SUB} is clearly the dominant component. More precisely, in the next sections, methods are reviewed to decreasing the sub threshold leakage currents in circuits that are in STANDBY or ACTIVE state.

III LEAKAGE POWER REDUCTION TECHNIQUES

Devices which are operated on battery are either Standby or Active mode. Leakage power can be divided in to two categories based on these two modes:

1 Leakage Control in Standby Mode: Techniques like Power gating and super cutoff CMOS are used for leakage reduction in standby mode. In these techniques, circuit is cutoff from the supply rails, when it is in idle state.

2. Leakage Control in Active Mode: Techniques like forced stacking and sleepy stack can be used during the run time or active mode for leakage current reduction.

This can be achieved by process and circuit level techniques. At the process level, this can be achieved by controlling the dimensions like length, oxide thickness and junction depth etc and doping profiles in the transistor. At the circuit level, threshold voltage and leakage current can be controlled by controlling the voltages of different device terminals (drain, source gate and body/substrate).

In Device-Level Leakage Reduction Techniques are:

1. Retrograde Doping **2.** Halo Doping

In Circuit-Level Leakage Reduction Techniques are:

1. Transistor Stacking **2.** By Input Vector Control

3. By Multiple Threshold Voltage Designs **4.** By Power Cut-Off

5. Dynamic Power Gating

Here various leakage reduction techniques reviewed in detail.

3.1. Sleep method

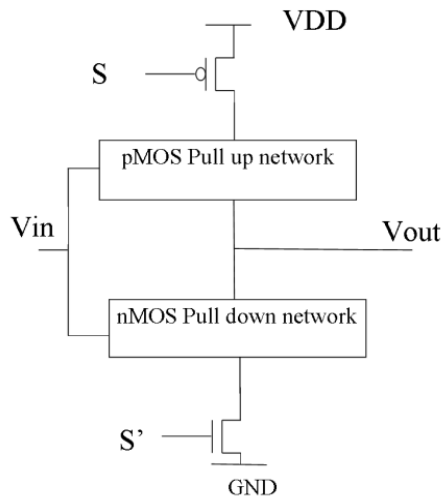

Figure 2. Sleep Transistor.

In case of sleep approach in fig.2, transistors gating VDD and GND are added to the base case. The added transistors cut off supply of power when in sleep mode. Each added transistor is referred to as “sleep transistor” and takes the width of the largest transistor in the base case. A PMOS transistor is placed between VDD and the

pull up network, and NMOS sleep transistor is placed between GND and pull down network. The sleep transistor turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively. The disadvantage in sleep approach is destruction of state and floating outputs.

3.2. Stack Approach

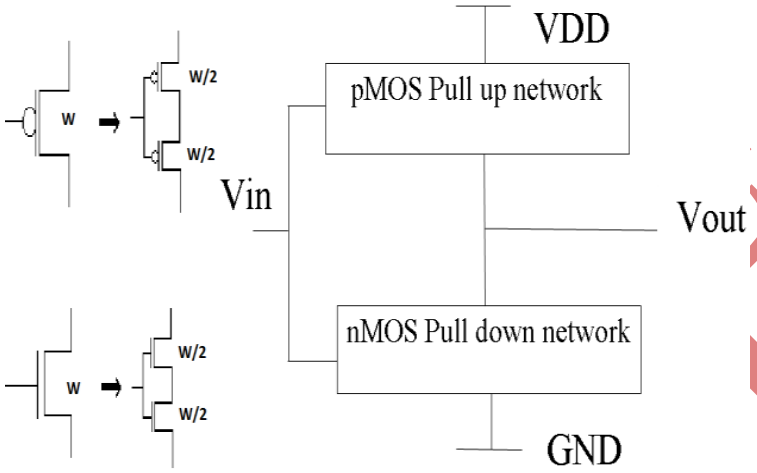

Figure 3. Stack Approach Structure.

The stack approach in fig.3 is based on the fact that natural stacking of MOS-FET helps in achieving leakage current. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect. An effective way to reduce leakage power in active mode is stacking of transistor .In this technique we have floating values and thus will lose state during sleep mode. The Wakeup time and energy of the sleep technique have significant impact.In this technique every transistor in logic network using CMOS logic is duplicated with both original and duplicate bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because subthreshold current is exponentially dependent on gate bias, a Substantial current reduction is obtained. As all transistors are placed in between two parallel rows of continuous VDD and GND, stack approach design forces an increase in row length because of an increase in number of transistors and decrease in transistor width. Even though state saving is done in stack approach delay is increased because of duplication of transistors.

3.3. Sleepy Stack

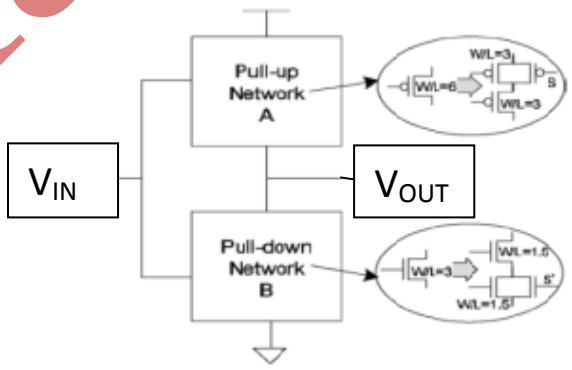

Figure 4. Sleep Stack Structure.

The sleepy stack approach in fig.4 combines the sleep and stack approaches as shown in fig.4. The sleepy stack technique divides existing transistors into two half Size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Sleep transistors are placed in parallel to the divided transistor closest to VDD for pull-up and in parallel to the divided transistor closest to GND for pull down. The sleepy stack approach can have advantages of both the stack approach and the sleep approach. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors. The above approach reduces static power and the output voltage levels stay in the defined ranges of logic-1 and logic-0, but circuit complexity increases as the number of transistors increase which also increases the area.

3.4. Sleepy Keeper

Solution against all the drawbacks in the previous techniques is presented in this section. This is a new leakage reduction technique which is called as the sleepy keeper in fig.5. The basic problem with traditional CMOS is, the transistors are used only in their most efficient and natural inverting way i.e. PMOS transistor is connected to VDD and NMOS transistor is connected to GND. It is well known that PMOS transistors are not efficient at passing GND i.e. weak zero output we are going to get. Similarly it is well known that NMOS transistors are not efficient at passing VDD i.e. weak one is the output form. However to maintain the value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor is connected to VDD to maintain output value equal to '1' when in sleep mode.

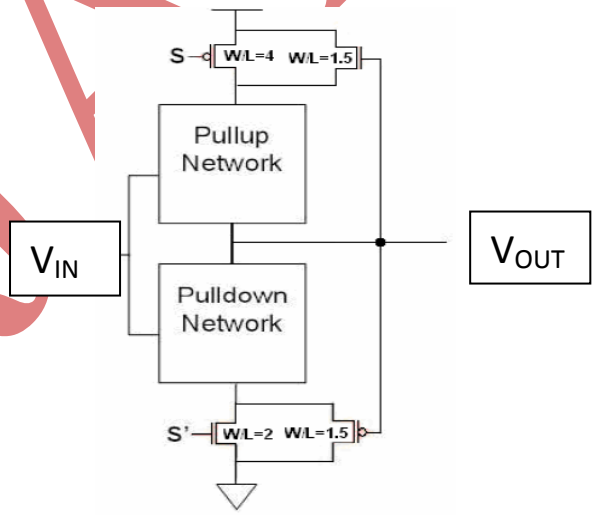

Figure 5. Sleepy Keeper Structure.

As shown in fig.5, an additional single NMOS transistor placed in parallel to pull-up sleep transistor connects VDD to pull up network. When in sleep mode, this NMOS transistor is only source of VDD to the pull-up network since the sleep transistor is off. Similarly to maintain a value of '0' in sleep mode, given that the '0'

value has already been calculated, the sleepy keeper approach uses this output value of '0' and PMOS transistor connected to GND to maintain output value equal to '0' when in sleep mode.

As shown in fig.5, an additional single PMOS transistor placed in parallel to the pull-down sleep transistor is only source of GND to the pull-down network which is the dual case of the output '1'. Sleepy keeper technique uses the traditional sleep transistors with two additional transistors to save state during sleep mode. Dual threshold voltages can also be applied in the sleepy keeper approach to reduce sub threshold leakage current.

IV CONCLUSION

With the continuous technology scaling devices, the leakage power is of great concern for designs in nanometer technologies and is becoming a major contributor to the total power consumption; leakage power has become more dominant as compared to Dynamic power. The gate leakage has become dominant sources of leakage and is expected to increase with the technology scaling. The solutions for leakage power dissipation or reduction of leakage power dissipation have to be sought both at the process technology and circuit levels. Here we thoroughly reviewed the some of the techniques efficiently used in reducing leakage power consumption in all digital as well as analog designs.

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