DESIGN AND ANALYSIS OF SUB 1-V BANDGAP REFERENCE (BGR) VOLTAGE GENERATORS FOR PICOWATT LSI's.

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ABSTRACT

A bandgap reference (BGR) and sub–1V BGR circuits for Picowatt LSIs is proposed here. The circuits pertains pico-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. The circuits neglect resistors and contain only MOSFETs and one bipolar transistor. As the sub-BGR circuit divides the output voltage of the bipolar transistor without resistors, it can operate at a sub–1V supply. Experimental results obtained in the 90nm CMOS technology depicts that the BGR circuit could generate a reference voltage of 1.094 V and the sub-BGR circuit could generate one of 0.549 V. The power dissipations of the BGR and sub-BGR circuit corresponds to 8.466 PW and 3023 PW.

Keywords: (Sub) Bandgap Reference, Low Voltage, Large Scale ICs (LSI), Multi-Threshold Devices, Picowatt.

I INTRODUCTION

The objective of this paper is to design picowatt LSIs that will lead the next generation power efficient applications like wireless sensor networks, metrological sensors, life-assist medical devices. Since they must operate for a long time with less-than-ideal energy supply from micro-batteries, we thus require the LSIs such designed that operate with extremely low power dissipation. To develop such LSIs, we must first develop voltage reference circuits because they are the building blocks of most analog circuits. Bandgap reference (BGR) circuits are widely used in modern LSIs to generate a reference voltage on chips. Here, we describe process, voltage, and temperature (PVT) variation-tolerant voltage reference circuits that can operate at several tens of picowatts or even less. The base-emitter voltage V_{BE} of the bipolar transistor is accepted by voltage divider circuit which generates a sub−1V reference voltage in combination with the PTAT voltage generators. Although several BGRs have been developed until now, still the power dissipations of most of them exceeds picowatt power units [1]–[2] and have not been significantly reduced.This is due to the use of resistors in the circuits. In reference circuits, the resistors are mostly

used to generate current or voltage to control the temperature characteristics of the output reference voltage [1]–[3]. We use a moderate value for resistance, still a sufficient current for the resistors is required and therefore , power dissipation cannot be reduced. Although it can be reduced if we use a large value for resistance, but then the resistors will occupy a large silicon area which is not considered fruitful. Our circuit avoids the usage of resistors and contains only MOSFETs and one bipolar transistor. A resistor-less voltage reference circuits that operates at picowatt power have been used. The proposed BGR consists of a pico-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. Because the circuit only consists of MOSFETs except for the bipolar transistor, it can generate a bandgap voltage without resistors. In addition, a sub-BGR circuit that generates voltage lower than 0.549 V is also presented. The proposed sub-BGR uses a voltage divider. The voltage divider accepts the base-emitter voltage of the bipolar transistor and generates a sub−1V reference voltage in combination with the PTAT voltage generators. Therefore, the proposed sub-BGR is useful as a reference circuit in sub−1V LSIs. Any additional devices, such as passive resistors, are not anymore needed in the circuit. For the robust operation of the circuit, we used pico-ampere current reference circuit that is tolerant to PVT variations. Section II of this paper describes the operating principles of our proposed circuits. Section III describes the implementation of both circuits using 90nm CMOS process technology and presents the experimental results by comparing it with experimental results of 180nm CMOS process technology. An extremely low power dissipation of 8.466 PW for the BGR and 3023 PW for the sub−1V BGR were achieved. Section IV concludes the paper.

II OPERATING PRINCIPLES

2.1 Current in Subthreshold Region

The subthreshold current I, can be expressed as

$$I = KI_0 \exp((V_{GS}-V_{TH})/\eta V_T), \quad (1)$$

where K (= W/L) is the aspect ratio of a transistor, I_0 (= $\mu C_{OX}(\eta-1)V^2_T$) is the pre-exponential factor of the subthreshold current, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T (= k_BT/q) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, V_{TH} is the threshold voltage, and η is the subthreshold slope factor. Note that, we assumed that η is a constant parameter. However, it is not constant in actual devices and depends on gate-oxide and capacitances of depletion-layer [4]. This must be taken into account in high-accuracy applications.

2.2 BGR

Figure 1 shows the architecture of the proposed BGR circuit.

Bandgap Voltage References find its applications in data acquisition systems. Ideally, this block will supply a fixed dc voltage of known amplitude that does not change with temperature. There have been number of approaches that have been taken to realize voltage references in integrated circuits. These include:

1. Making use of a zener diode that breaks out at known voltage when reversed biased.

2. Making use of difference in the threshold voltage between an enhancement transistor and a depletion transistor.
3. Cancelling the negative temperature dependence of a pn junction with positive temperature dependence from a PTAT (proportional-to-absolute- temperature) circuit.

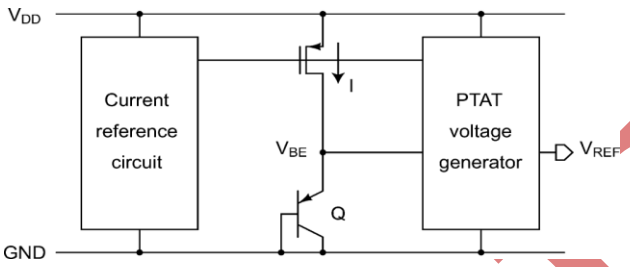
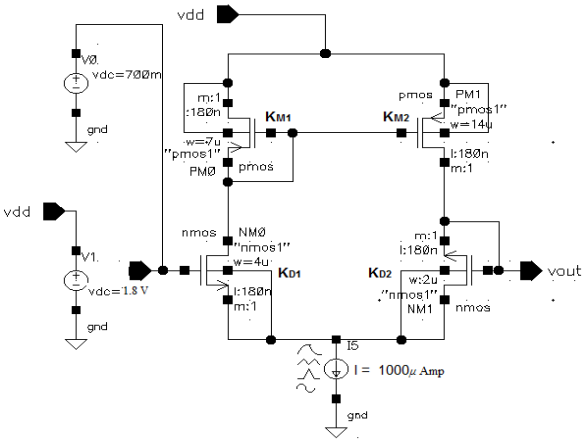


Fig. 1: Architecture of the Proposed BGR Circuit.

The first approach is not popular nowadays because the breakdown voltage of a zener diode is typically larger than the power supplies used in modern circuits. The second approach cannot be used in most CMOS circuits because depletion transistors are not typically available. In addition, although it can be used to make quite stable references, the actual value of references is difficult to determine accurately because of the process sensitivity of the difference between the threshold voltage of an enhancement device and a depletion device. For the reasons, the first two approaches are not covered here. Rather, the last approach is discussed. Voltage references based on the last approach are called "bandgap" voltage references for a reason that becomes apparent shortly. A resistor-less proposed circuit of BGR consist of PTAT voltage generators**,** one bipolar transistor, a pico-ampere current reference circuit. PTAT voltage generator consist source-coupled differential pairs and generates a positive temperature dependent voltage that compensates for negative temperature dependence of a base-emitter voltage in p-n-p bipolar transistor to maintain accuracy. Any additional devices like passive resistors are not anymore needed in the circuits. Figure 2 shows the architecture of the PTAT voltage generator consisting of differential pair circuit



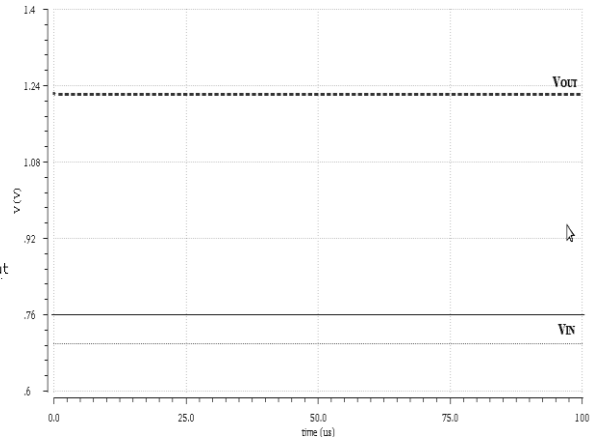


Fig. 2: Architecture of the PTAT circuit **Fig. 3: Measured output voltage of PTAT circuit**

When the MOSFETs operate in the subthreshold region, gate-to-gate voltage V_{GG} in this circuit can be expressed from (1) as

$$V_{GG} = V_{OUT} - V_{IN}$$
$$= [\, V_{TH} + \eta V_T \ln (I_{D2}/K_{D2}\, I_0)] - [(V_{TH} + \eta V_T \ln (I_{D1}/K_{D1}\, I_0)]$$
$$= \eta VT \ln (K_{D1}\, K_{M2} / K_{D2}\, K_{M1}) \quad (2)$$

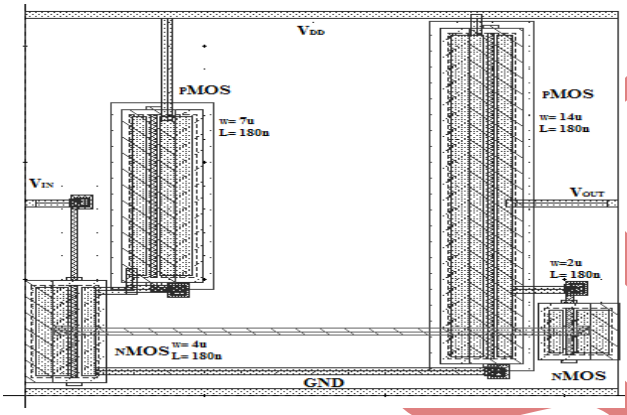


Fig. 4: Layout of PTAT Voltage generator

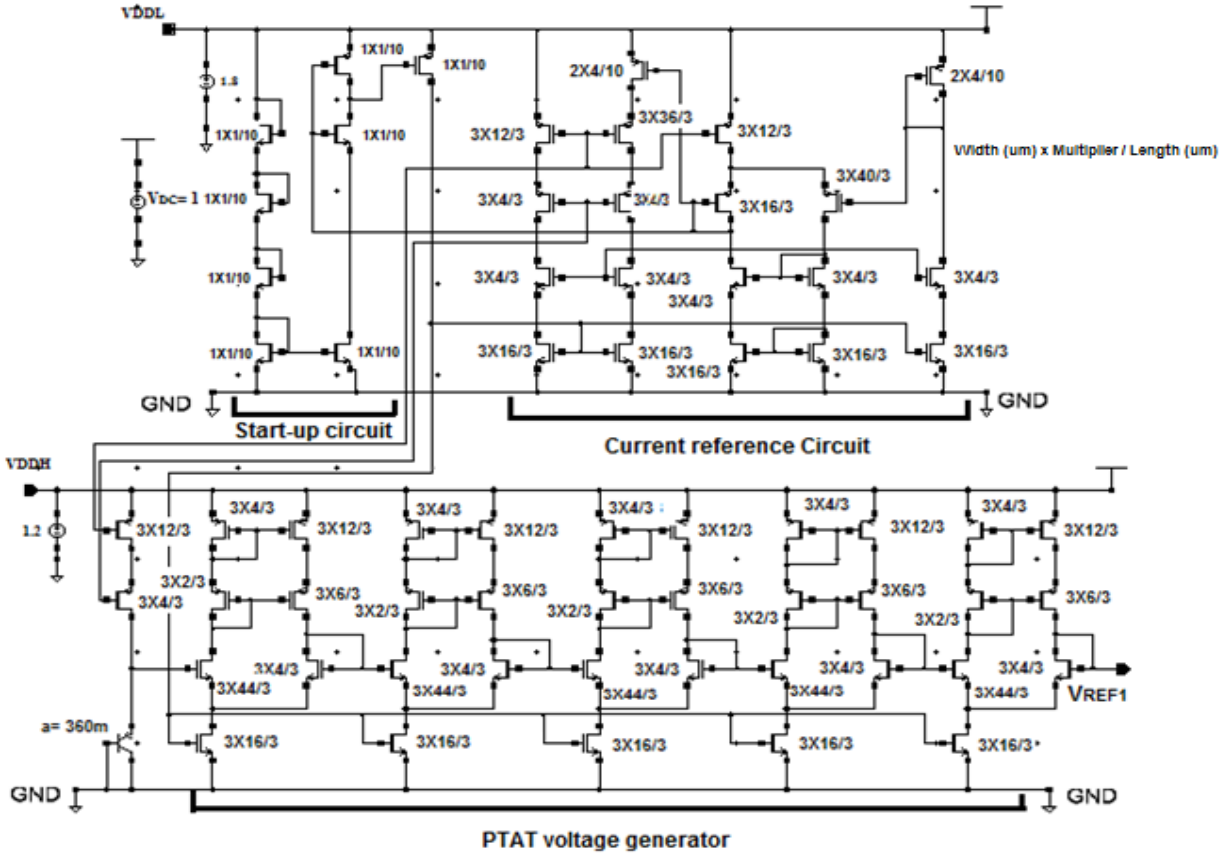


Fig. 5: Schematic of proposed BGR Circuit in 90nm Technology

To operate the circuits robustly, we used a pico-ampere current reference circuit that is tolerant to PVT variations. We ignore the gate and substrate leakage currents since they are negligible when compared to sub-threshold current. Therefore, the bandgap voltage of silicon can be obtained by designing aspect ratios in the source-coupled pairs. The bipolar transistor accepts the current through a current mirror and generates a base-emitter voltage, which is expressed as

$$V_{BE} = V_T \ln (I_S + I)/ I_S \quad (3)$$

Where I_S is the saturation current of the bipolar transistor. Since V_{BE} decreases linearly with temperature, (3) can be simplified as

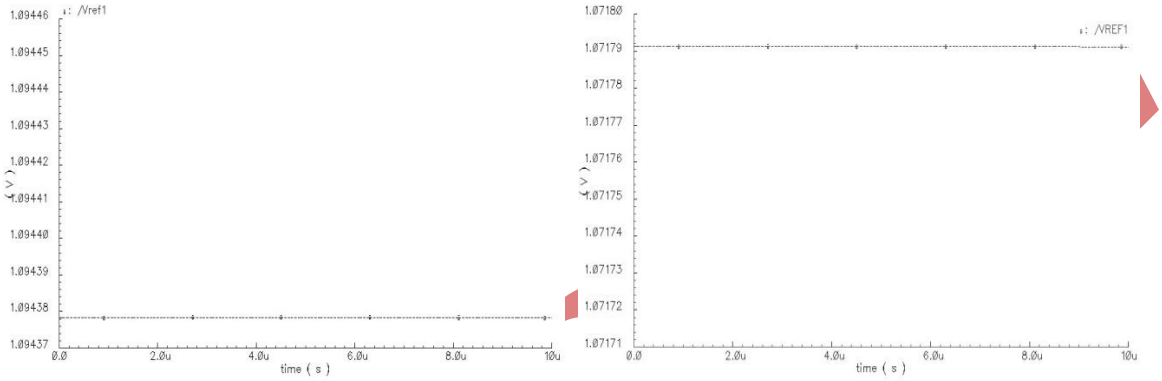


Fig 6: V_{REF1} of proposed BGR Circuit in 90nm Tech. Fig 7: V_{REF2} of modified BGR Circuit in 180nm Tech.

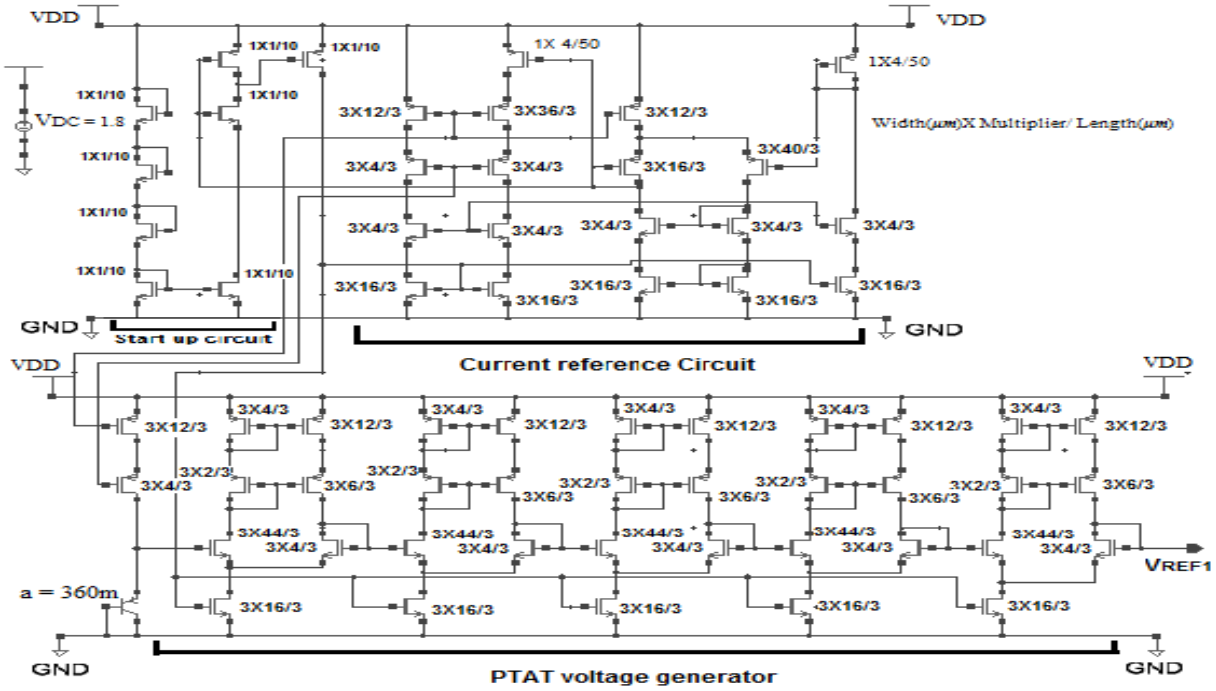


Fig. 8: Schematic of modified BGR Circuit in 180nm Technology

Where V_{BGR} is the bandgap voltage of the silicon (~ 1.2 V) and y is the temperature coefficient of V_{BE}. Because V_{BE} has a negative dependence on temperature, the PTAT voltage generator is used to cancel out this dependence. Since V_{BE} has a higher order dependency on temperature. So, there will be nonlinearities in the output voltage even though we cancel out the negative dependence of V_{BE} on temperature. The PTAT voltage generator in Figure 2 supplies voltage which has a positive dependence on temperature. But, since $K_{D1}K_{M2}$ / $K_{D2}K_{M1}$ is included in a logarithmic function, it must have a large value in order for the positive temperature coefficient of V_{GG} to cancel out the negative temperature dependence of base-emitter voltage V_{BE}. Moreover, making the product of $K_{D1}K_{M2}$ much larger requires a large area and which cannot be made use of efficiently. We, thus use a number of differential pairs in cascade configuration to obtain sufficient PTAT voltage. When the differential pairs are connected in a cascade, total gate-to-gate voltage V_{GG} can be expressed as

$$\sum_{i=1}^{N} V_{\mathrm{GG},i} = \sum_{i=1}^{N} \eta V_T \ln\left(\frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}}\right)$$
$$= \eta V_T \ln\left(\prod_{i=1}^{N} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}}\right) \quad (5)$$

Where N is the number of differential pairs. Output reference voltage V_{REF1} in the bandgap voltage reference circuit can be expressed from (4) and (5) as

$$V_{\mathrm{REF1}} = V_{\mathrm{BE}} + \sum_{i=1}^{N} V_{\mathrm{GG},i}$$
$$= V_{\mathrm{BGR}} + \left(-\gamma + \eta\frac{k_B}{q} \ln\left(\prod_{i=1}^{N} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}}\right)\right) T. \quad (6)$$

Therefore, the condition V_{REF1} equals to V_{BGR} can be attained by appropriate choice of the aspect ratios of the transistors in the differential pairs and current mirrors and of N. Also multi-threshold (MTCMOS) voltage supplies are provided to the BGR circuit by applying different bias voltages to base/bulk terminal so as to optimize the power. Although, the low threshold devices cause faster switching but it causes static leakage power. The high threshold devices cause ten times reduction in static leakage power.

2.3 SUB BGR

Figure 9 shows the architecture of the proposed Sub-BGR circuit.

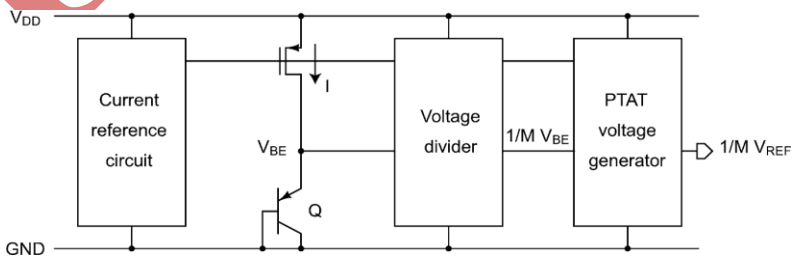


Fig. 9: Architecture of the proposed BGR circuit

Here, we present a voltage reference circuit that operates at sub−1V power supply. This sub-BGR circuit uses an extra voltage divider block. The voltage divider circuit divides the base-emitter voltage V_{BE}. The output voltage V_{BE}/M of the voltage divider can be expressed as

$$V_{BE}/M = V_{BGR}/M - y/M\ T \quad (7)$$

where M is the division ratio of the divider. The PTAT voltage generator is also used to cancel the negative dependence on temperature of V_{BE}/M. The reference output voltage of this circuit is expressed as

$$V_{REF2} = \frac{V_{BGR}}{M} + \left(-\frac{\gamma}{M} + \eta\frac{k_B}{q} \times \ln\left(\prod_{i=1}^{N'} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}}\right)\right) T \quad (8)$$

where N′ is the number of differential pairs. Note that because base-emitter voltage V_{BE} is divided by M, the negative temperature coefficient is also divided by M. Hence, the required PTAT voltage decreases and the number of differential pairs are also reduced as compared to BGR circuit. Thus, both the area and the current dissipation in the sub-BGR circuit are less than those in the BGR circuit. A zero temperature coefficient voltage is obtained by designing the aspect ratios so that the second term in (8) becomes zero and the voltage can be rewritten as

$$V_{REF2} = V_{BGR} / M \quad (9)$$

III EXPERIMENTAL RESULTS

3.1 Circuit Implementation

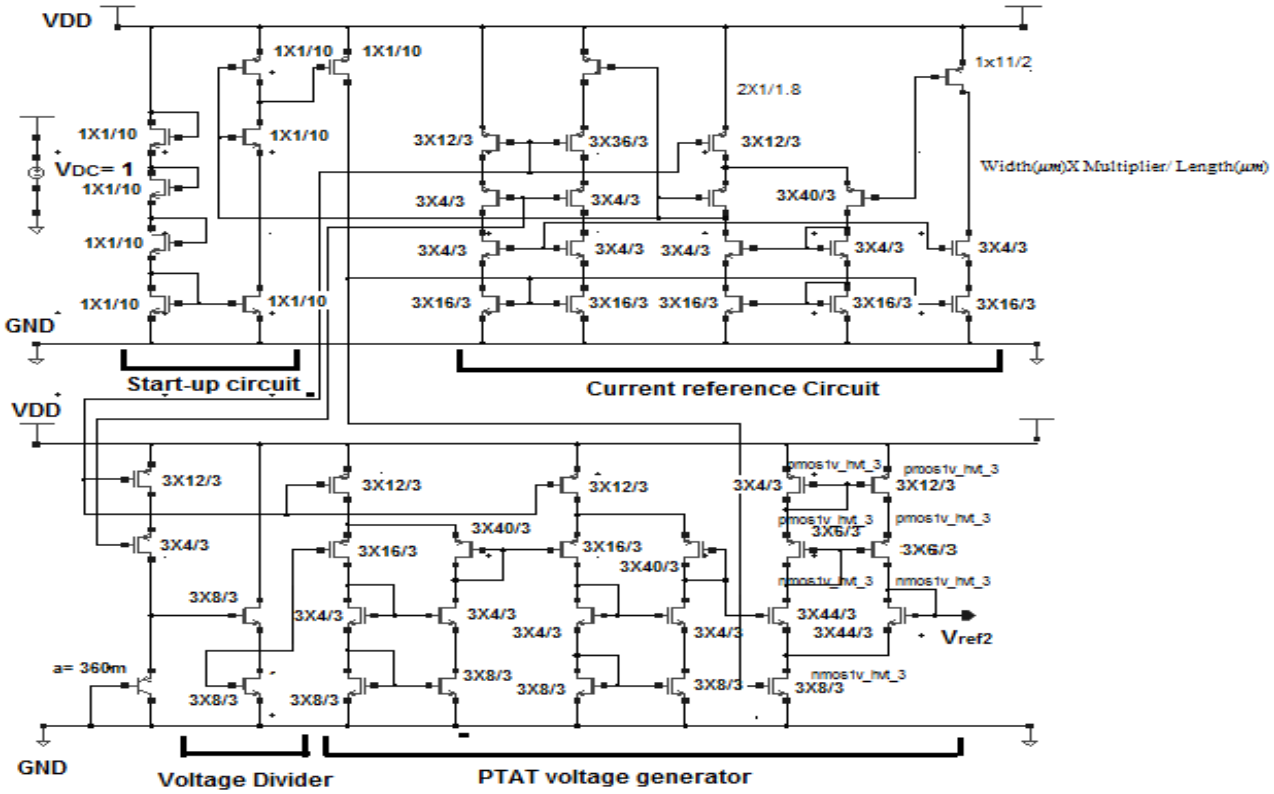


Figure 5 and 10 shows the schematics for the proposed BGR and sub-BGR circuits with all transistor sizes. As explained earlier, cascode configuration was used in the circuits to reduce dependence on supply voltage. Five differential pairs were used in this BGR design. The reference output voltage V_{REF1} of this circuit can be expressed as

$$V_{\mathrm{REF1}} = V_{\mathrm{BGR}} + \left(-\gamma + \eta\frac{k_B}{q}\ln\left(\prod_{i=1}^{5}\frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}}\right)\right)T. \quad (10)$$

A zero temperature coefficient voltage can be obtained by designing the aspect ratios in the differential pairs and the current mirrors so that the second term in (10) becomes zero. We used a source-follower circuit as a voltage divider circuit in the sub-BGR. The voltage divider circuit divides the base emitter voltage V_{BE} in half. Each body terminal of the pMOS-FETs in the source-follower circuit was connected with their source terminal to avoid the body effect of the transistor. We ignored the gate and substrate leakage currents because these leakage currents were smaller than the sub-threshold current in the process we used.

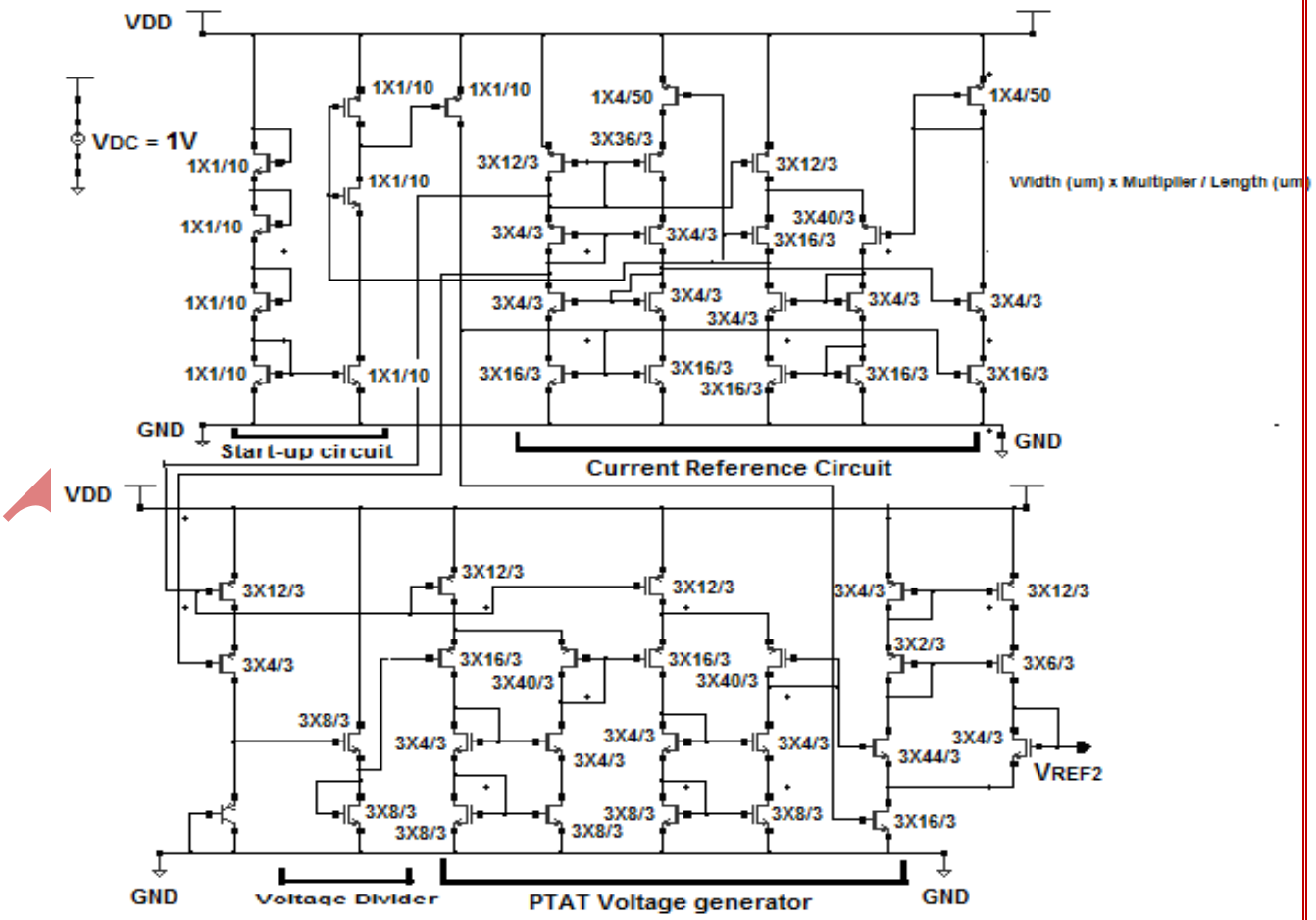


Fig. 11: Schematic of modified sub-BGR circuit in 180nm technology.

The output voltage $V_{BE}/2$ of the source-follower circuit can be expressed as

$$V_{BE}/2 = V_{BGR}/2 - y'/2\ T \quad (11)$$

Then, three differential pairs were used in the sub-BGR to cancel the negative dependence on temperature of $V_{BE}/2$. We used two pMOS differential pairs as first PTAT voltage generators because $V_{BE}/2$ would have been too low to apply an nMOS PTAT generator. The reference output voltage V_{REF2} of this circuit can be expressed as

$$V_{REF2} = \frac{V_{BGR}}{2} + \left(-\frac{\gamma}{2} + \eta_P \frac{k_B}{q} \ln \left(\prod_{i=1}^{2} \frac{K_{D2i-1} K_{M2i}}{K_{D2i} K_{M2i-1}} \right) + \eta_N \frac{k_B}{q} \ln \left(\frac{K_{D5} K_{M6}}{K_{D6} K_{M5}} \right) \right) T. \quad (12)$$

Therefore, a zero temperature coefficient voltage can be obtained by designing the aspect ratios in the differential pairs and the current mirrors so that the second term in (12) becomes zero and the voltage can be rewritten as

$$V_{REF2} = V_{BGR}/\ 2 \quad (13)$$

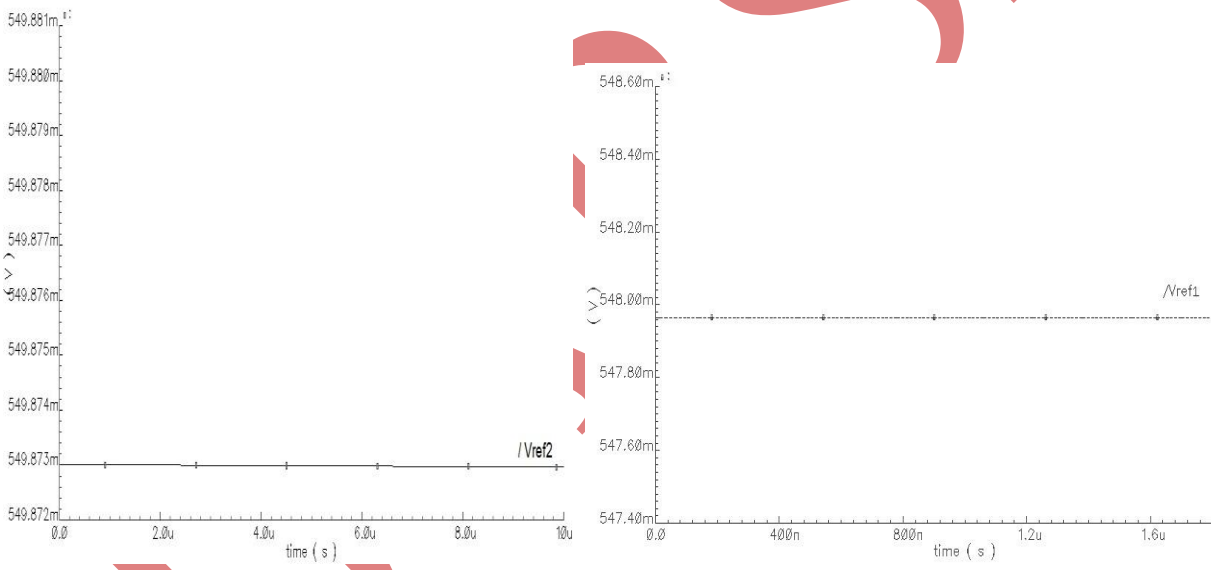


Fig. 12: Voltage Output of proposed Sub BGR Circuit in 90nm technology.

Fig. 13: Voltage Output of modified Sub BGR Circuit in 180nm technology

3.2 RESULTS

Figure 14 plots the measured operating current in the current reference circuit as a function of V_{DD} for sub-BGR circuit in 90nm technology. The circuit operates at 1V power supply The BGR circuit generated V_{REF1} as 1.09 V at more than 1.2 V power supply. The sub-BGR circuit could operate at sub−1V power supply (i.e., 0.7 V) and V_{REF2} was 0.549 V. Figure 15 plots the measured voltages of V_{REF2} as a function of temperature from 0°C to 100°C for 90nm technology.

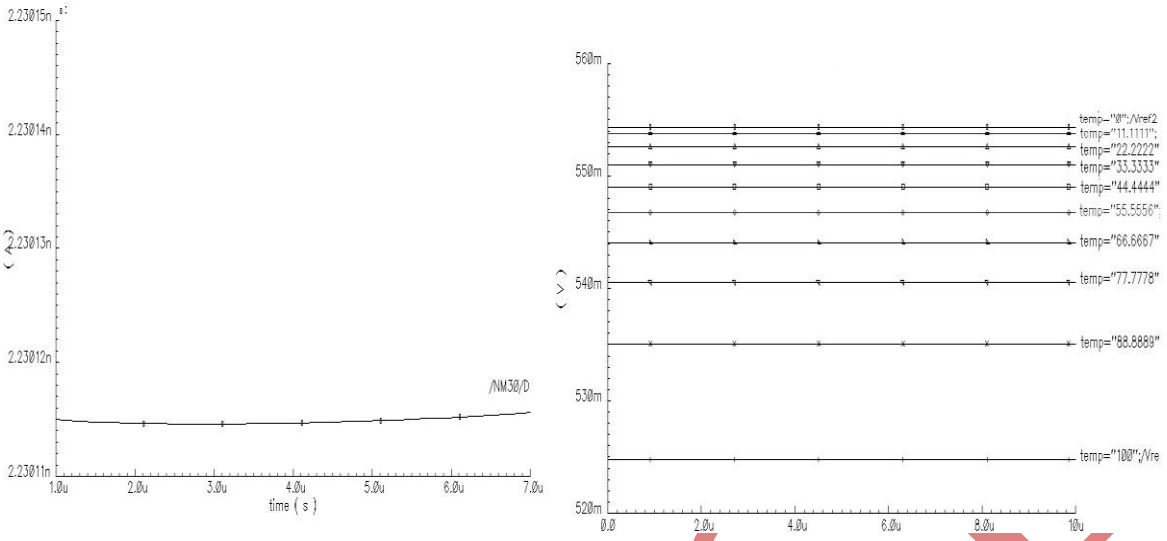


Fig. 14: Measured Operating Current of Sub-BGR circuit in 90nm Technology

Fig. 15: Measured Voltage of V_{REF2} as a function of ten various temperature values

	[1] Proposed		[2] Modified	
CMOS Technology	90nm		180nm	
Circuit Type	BGR	Sub-BGR	BGR	Sub-BGR
Supply Voltage (V)	1	1	1.8	1.8
Transition Time (µs)	10	1.6	10	1.6
Reference Voltage V_{REF} (V)	0.548	0.549	1.071	1.094
Temperature (°C)	0–100	0–100	– 40-120	– 40-120
Power Dissipation (W)	8.466 PW	3023 PW	60.23 NW	38.38 NW

TABLE 1: EXPERIMENTAL RESULTS AND COMPARISON

Table 1 summarizes the performance of the proposed BGR and sub-BGR circuits using 90nm CMOS process technology and presents the experimental results by comparing it with experimental results of modified 180nm CMOS process technology.

3.3 Discussion

Output voltage V_{REF1}, 1.09 V, in the experimental results was lower than the material bandgap voltage, around 1.2 V. This is because the operating current increases with temperature. If bipolar transistor accepts the constant currents, then the V_{BE} at absolute zero temperature were almost equal to the material bandgap voltage (~1.2 V). On the other hand, when the bipolar transistor accepts the temperature-dependent current, then the V_{BE} at absolute zero temperature is not equal to the material bandgap voltage. As the operating current increases with temperature, V_{BE} increases gradually. As a result, V_{BE} at absolute zero temperature became lower than the material bandgap voltage.

IV CONCLUSION

BGR and sub–BGR circuits for Picowatt power LSIs were presented. They consist of a pico–ampere current reference circuit, a bipolar transistor, and PTAT voltage generators. Because the circuits only consist of MOSFETs except for the bipolar transistor, they generate reference voltages without resistors. As the sub-BGR circuit divides the output voltage of the bipolar transistor, it can operate at sub–1V power supply. The experimental results demonstrate that the PTAT Voltage Generator circuit has voltage output of 1.26 V. The BGR and sub- BGR circuit could generate a reference voltage of 1.094 V and 0.549 V respectively. The power dissipation of the BGR circuit was 8.466 pW and that of the sub-BGR circuit was 3023 pW.

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