INFLUENCE OF HETEROGENEOUS GATE DIELECTRIC ON HETERO-DIELECTRIC-DMG-GAA-TFET FOR IMPROVED TUNNELING CURRENT

Jaya Madan[1], R.S. Gupta[2], Rishu Chaujar[3]
[1]*Department of Engineering physics, DTU, Delhi (India)*
[2]*Professor & Head in Department of ECE, MAIT, Delhi (India)*
[3]*Assistant Professor, Department of Engineering physics, DTU, Delhi (India)*

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ABSTRACT

In this paper, we propose and validate a Heterogate Dielectric- Dual Material Gate-Gate All Around, Tunnel Field Effect Transistor (HD-DMG-GAA-TFET). A comparative study for different values of high-k has been done, and it has been clearly shown that the problem of lower I_{ON} (which hinders the circuit performance of TFET) can be overcome by using the dielectric engineered hetero-gate architecture. The HD-DMG-GAA-TFET shows an enhanced I_{ON} of the order of 10^{-4}A and an I_{ON}/I_{OFF} of the order of 10^{12} (approximately). The perfect saturation of drain current is obtained and hence the device is a worthy candidate for sub nanometre range, for low power analog application. Further, the comparison of the proposed device with conventional Gate All Around Tunnel Field Effect Transistor (GAA-TFET), has been done and it has been found that the proposed device has greater tunneling current driving capacity.

Keywords- Ambipolarity, ATLAS-3D, band to band tunneling (BTBT), barrier width, heterogate dielectric, high-k, subthreshold swing (SS), TFET (tunneling field effect transistor).

I. INTRODUCTION

The miniaturizing of semiconductor devices for increasing the speed of the device, decreasing the area occupied and power consumed by the circuit results into increase in leakage currents, short channel effects and static power consumption for the integrated circuits. Numerous kinds of novel electron devices have been introduced to overcome the scaling limit of MOSFETs [1-3]. But all the MOSFETs use the diffusion over the thermal barrier and hence have a fundamental limit of (KT/q).ln10~60mV/dec; which leads to increase in static power consumption. Hence, the devices which use a new carrier transport mechanism other than diffusion over a thermal barrier came into existence. Among these devices, Tunnel Field Effect Transistor (TFET), which uses a band to band tunneling (BTBT) mechanism; to overcome this fundamental limit of subthreshold swing, acts as a promising candidate for further extending the Moore's law. Due to its immunity to short channel effects, lower subthreshold swing (SS) and lower off current (I_{OFF}), TFET is found to be the potential candidate to replace the MOSFET [4-6]. Due to lower I_{OFF} of the TFET, switching characteristics of TFET are far better than MOSFET. The major challenge in adopting TFET for wide scale application is its lower I_{ON}; in order to tackle this problem many novel device designs and materials such as double-gate, delta layer, SiGe, and

PNPN structures have been proposed [7-11]. To enhance I_{ON}, a high-k material has been locally inserted (near the source side) in the gate dielectric to form heterogate-dielectric (HD) TFETs [12]. In HD-TFETs the gate dielectric is split into two regions; high-k dielectric near the source side and low-k dielectric near the drain side The presence of high-k results into a higher band bending due to increase in surface potential (at a constant gate bias) [13]. Another practical problem that needs to be tackled with TFET is high threshold voltage. To resolve this issue many structures were proposed such as, tunnel bandgap modulation, gate work function engineering, vertical tunnel field effect transistor (TFET) with SiGe delta doped layer, and high-k gate dielectric with double gate, higher source doping and abrupt doping profile [14-19]. Another major problem with TFET is ambipolarity. The ambipolarity in the device is the conduction for both high positive and high negative V_{GS}, while keeping the V_{DS} only in one direction (negative for p-type devices and positive for n-type devices) [20]. A higher ambipolar behaviour deteriorates the SS and standby power consumption of devices. When a high-k material is applied to the entire gate dielectric ambipolar behaviour increases, and hence causes a higher OFF current. This ambipolarity effect can be reduced by using a hetero gate dielectric structure. The higher value of dielectric improves the electrical coupling between the gate and the tunneling junction (the source-channel junction) and hence, increases the tunneling rate. The dual material gate further helps in the improvement of ON/OFF characteristics. Lower work function metal near the source side, increases the band overlap and hence reduces the tunneling barrier width. This reduced tunneling barrier increases the tunneling probability and the generation rate which results in higher I_{ON} and the higher value of work function near the drain side increases the tunneling barrier width and hence helps in reducing the I_{OFF}. So an optimum value of metal work function value at source and drain side should be chosen to trade-off between ON and OFF characteristics. In this work, a heterogate dielectric, dual material gate, gate-all around (GAA) structure has been applied to TFETs with the aim of higher I_{ON} and to improve the device characteristics.

II. DEVICE STRUCTURE: PARAMETERS AND SIMULATION MODELS

The Gate All Around (GAA) geometry is considered with radius (R) of 10nm, channel length (L_g) of 50nm which is basically equal to the sum of length of region 1 and region 2 respectively (L_1 (20nm) and L_2 (30nm)), in case of HD-DMG-GAA-TFET and gate oxide thickness (t_{ox}) of 2nm. The source is p+ type doped ($1\times10^{20}cm^{-3}$) and drain is n+ doped (5×10^{18} cm^{-3}) and body is lightly p type doped ($1\times10^{16}cm^{-3}$). To reduce ambipolarity effect source and drain are doped asymmetrically. In case of HD-DMG-GAA-TFET region 1 consists of dielectric constant ε_1=21 (high-k) and metal work function Φ_{M1}=4.1eV (near the source) and region 2 consists of ε_2=3.9 (low-k) and Φ_{M2}=4.4eV (near the drain). While studying the effect of high-k ε_1=7.5, 21 and 29 corresponding to Si_3N_4, HfO_2 and ZrO_2 respectively and ε_2=3.9 (SiO_2) were used. In case of GAA-TFET the dielectric constant 3.9 and gate metal work function 4.1eV is used. The source and drain junctions are abruptly doped for an effective band to band tunneling. Fig.1 shows the simulation device structure i.e. HD-DMG-GAA-TFET consisting of heterogate dielectric and dual material gate. All simulations have been performed using the ATLAS device simulator. The models activated during simulation are as follows: concentration and field dependent mobility model, non-local band to band tunneling, Shockley-Read-Hall for carrier recombination, band gap narrowing and Fermi Dirac statistics [21].

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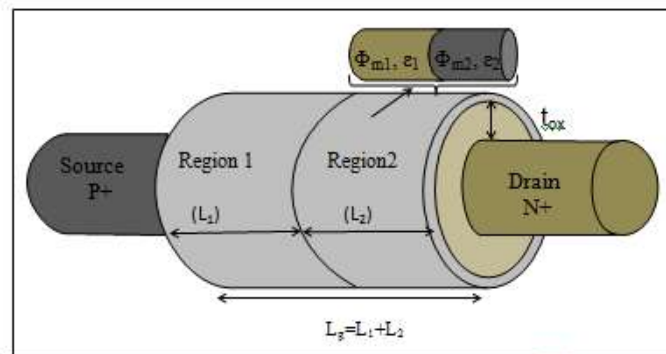

Fig.1: Structure of Heterogate Dielectric-Dual Material Gate-Gate All Around-Tunnel MOSFET (HD-DMG-GAA-TFET).

III. RESULT AND DISCUSSION

IMPACT OF HETERO-GATE DIELECTRIC

The drain current characteristics, transconductance, output characteristics have been studied and simultaneously the impact of high-k is considered. The presence of high-k near the source results into a higher band bending due to increase in surface potential (at a constant gate bias). The higher band bending results into reduction of tunneling barrier width, which further enhances the generation rate and hence the I_{ON}. It is evident from Fig.2 that among the three dielectric constants, the higher value of dielectric constant corresponds to higher current driving capability; this is because of the increase in band bending with higher dielectric constant, which reduces the tunneling barrier width and hence, enhances the generation rate. But the counter effect is the degradation of OFF characteristics; due to comparative higher band bending at higher gate dielectric resulting in tunneling of electrons at lower gate voltage. This results in higher leakage current which eventually results in higher static power dissipation. Hence we have to trade-off between I_{ON} and I_{OFF} to optimise the I_{ON}/I_{OFF} ratio and the subthreshold swing. The highest I_{ON}/I_{OFF} ratio is for Si_3N_4 (ε_1=7.5). Further it is evident that the GAA-TFET has 100 times lower I_{ON} as compared to HD-DMG-GAA-TFET. Transconductance g_m, or device gain which is basically the first order derivative of the drain current with respect to the gate voltage at constant drain bias, is shown in Fig.3. The peak of transconductance curve gives the optimum bias point if device is to be used as an amplifier. It clearly shows that among the three dielectric constants and GAA-TFET the gain of the device is higher for higher dielectric constant, due to the enhanced electrical coupling between the gate and the tunneling junction (the source-channel junction) with higher dielectric constant, which further enhances the tunneling rate.

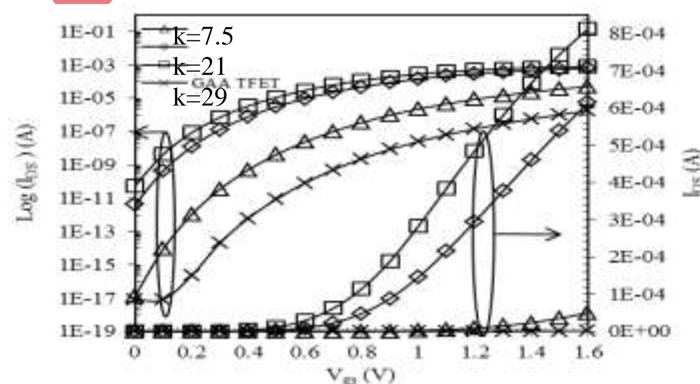

Fig.2: Drain current as a function of gate voltage (V_{GS}) for different values of high-k and for GAA-TFET at V_{DS}=0.8V.

Hence, the more number of electrons tunnel through the barrier which eventually leads to enhancement in drain current and transconductance. Fig.3 (inset) indicates the transconductance for GAA-TFET; clearly the gain is around 100 times lower as compared to HD-DMG-GAA-TFET.

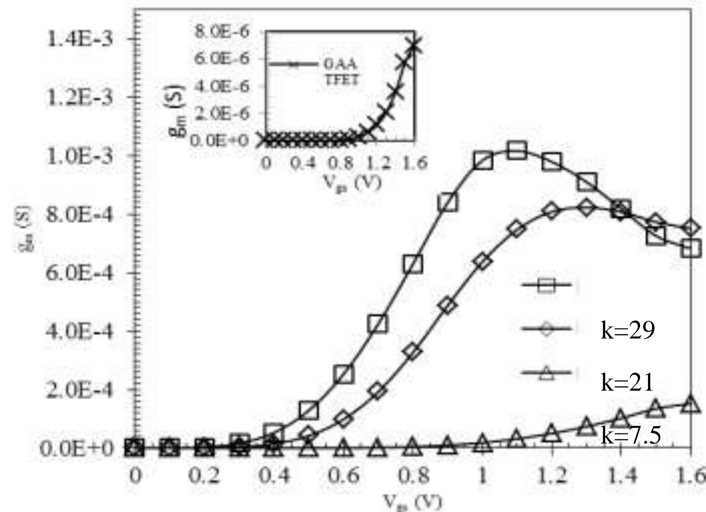

Fig.3: Transconductance as a function of gate voltage (V_{GS}) for different values of high-k and for GAA-TFET at V_{DS}=0.8V.

The output characteristic (I_{DS}-V_{DS}) at a constant V_{GS} = 1.0 V is illustrated in Fig.4. It is clear that the device predicts a qualitatively agreement in linear regime and also shows a well saturation in drain current for higher drain voltages. It has been obtained that the ZrO_2 has the better output characteristics as compared to Si_3N_4, HfO_2 and GAA-TFET. The output characteristics of GAA-TFET shown in Fig.4 (inset) for V_{GS}=1.0 V; Again the output current is much lower in case of GAA-TFET.

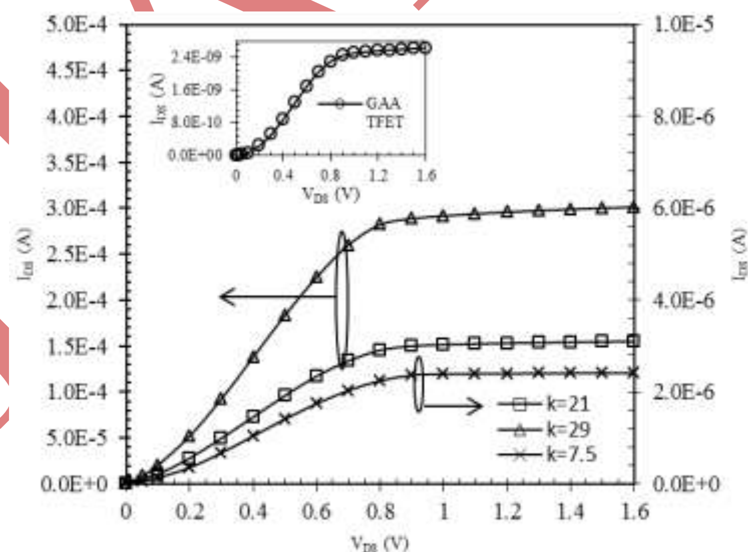

Fig.4: Drain current as a function of drain voltage (V_{DS}) for different values of high-k at V_{GS}=1.0 V and for GAA-TFET.

Output-conductance g_d, which is first order derivative of the drain current with respect to the drain voltage at a constant gate voltage, is shown in Fig.5. Again the output conductance has a higher peak for ZrO_2, increased by

an order of 100 (approximately) with respect to Si_3N_4. The output conductance for GAA-TFET is shown in Fig.5 (inset); g_d of GAA-TFET is manifold lower than that of HD-DMG-GAA-TFET.

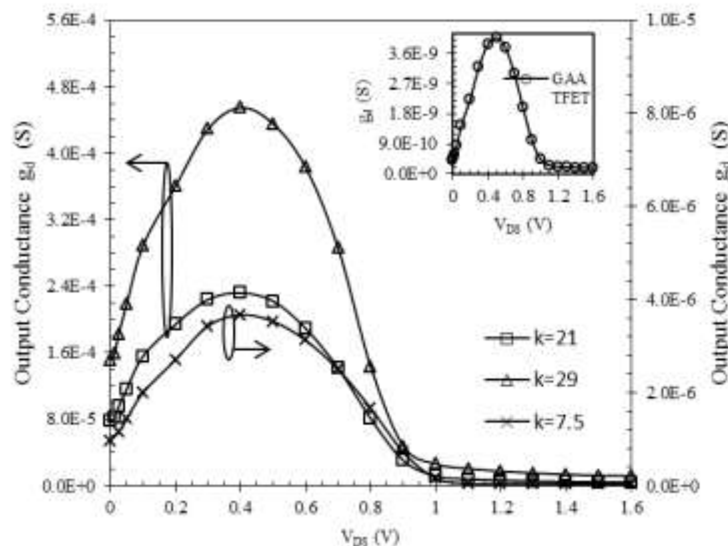

Fig.5: Output conductance as a function of drain voltage (V_{DS}) for different values of high-k and for GAA-TFET at V_{GS}=1.0 V.

IV. CONCLUSION

In conclusion the impact of high-k gate dielectric and comparison with GAA-TFET has been studied on the device performance. By using a high-k dielectric near the source side I_{ON} and transconductance has been enhanced. The output characteristic shows a very good saturation for higher drain bias. As in most of the conventional amplifiers, MOSFET is operated in saturation region or in linear region; therefore the device is well suited for analog applications and sub nanometre devices. But the counter effect of high-k is the degradation of OFF characteristics. Optimization of I_{ON}/I_{OFF} ratio depending on the application has to be done for sub nanometre devices. Both the static power dissipation and the higher I_{ON}/I_{OFF} ratio make the device an effective candidate for the analog application. While comparing the two devices; it is found that GAA-TFET has lower I_{ON} and device gain with respect to HD-DMG-GAA-TFET and hence HD-DMG-GAA-TFET is comparatively better candidate for analog performance.

V. ACKNOWLEDGMENT

The authors would like to thank to Microelectronics Research Lab, Department of Engineering Physics Delhi Technological University to carry out this work. Author would also like to thank University Grants Commission, Government of India, for the financial assistance during the course of this research work.

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Biographical Notes

Miss. Jaya Madan is presently pursuing Ph.D. in Engineering physics Department from DTU Delhi, India.

Dr. Rishu Chaujar is working as an Assistant Professor in Engineering physics Department, DTU Delhi, India.

Prof. R. S. Gupta is working as a Professor & Head in Department of ECE, MAIT, Delhi, India.

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