

CDTA BASED CURRENT MODE ADC

Neeta Pandey¹, Rajeshwari Pandey², Ranjana Sridhar³, Veepsa Bhatia⁴,
Alok Kumar Singh⁵, Pradeep Kumar⁶

^{1,2,3,4,5,6} *Department of Electronics and Communication Engineering
Delhi Technological University, Delhi, (India)*

ABSTRACT

This paper presents a CDTA based current mode analog to digital converter which shows the usefulness of CDTA as a building block in ADC design. The circuit is simple and is suitable for IC implementation as no external resistors or capacitors are required. The functionality of the circuit is verified with SPICE simulation using 0.35 μm CMOS technology parameters.

Keywords: Active Block; CDTA; Current Mode; Comparator; Flash ADC

1 INTRODUCTION

Signal processing is an important part of myriad systems around us. The input signals be they speech, temperature, voltage, current etc. are in analog form and can be processed directly. But with the advent of digital signal processing two main advantages could be had: higher accuracy and faster processing of complex manipulations. Digital signal processing is a critical part diverse system like telecommunication, audio processing, medical diagnostic imaging, function generation etc.

In digital signal processing or other digital instruments, sensors measure process variables which are in the form of analog signals. Then an electronic circuit, termed the analog-to-digital converter (ADC), converts the analog signals into equivalent digital representation of required accuracy that can be stored and processed. The overall speed and accuracy of the digital signal processing system is influenced by the speed and accuracy of analog to digital conversion as processing is carried generally on high speed special purpose microprocessor or microcontroller. Thus, the design of an ADC is very crucial as it determines the speed, accuracy, power dissipation of the digital signal processing system.

These days, current mode circuits are gaining popularity because of the advantages offered such as wider bandwidth and the capability for working under low voltage [1]. Most modern designs employ voltage mode elements like op-amps for implementation of various electronic circuits. These elements are used widely due to their small sizes and good performance. With the demand for portable battery powered equipment increasing, designers have begun to look into different architectures to fit these demanding designs. This issue is not easily solved with voltage mode elements since the voltage supply if reduced will cause problems with realizing good, fully-functional circuits. Instead, current mode (CM) elements are now being considered for the same circuits and these issues can then be addressed.

In this paper we present the design of a current mode ADC using the recently introduced active building block (ABB) current differencing transconductance amplifier (CDTA). The CDTA is characterized by large bandwidth and close-to-ideal terminal impedances. CDTA is a versatile sub circuit like the op-amp whose use in variety of applications in current mode signal processing, sinusoidal oscillators [2-13] has been explored. But, CDTA has not been used in applications like current mode ADCs and hence to check its viability, the paper focuses on this aspect. Section II discusses the basics of CDTA followed by Section III which enumerates the concept of CDTA based ADC. In Section IV, simulation results are presented followed by conclusion.

II CDTA BASICS

The circuit symbol of the CDTA is shown in Fig. 1 and the corresponding CMOS implementation in Fig. 2 [14] respectively. For Fig. 1, the terminal relationships can be described as $V_p=V_n=0$, $I_z = I_p - I_n$, $I_{x+} = g_m V_z$, $I_{x-} = -g_m V_z$, where V_p , V_n , V_x and V_z are the voltages at p, n, x and z terminals respectively, I_x is the output current at x terminal, I_0 is the input bias current and g_m represents transconductance. Here, from output terminal x, currents are equal in magnitude, but they flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes.

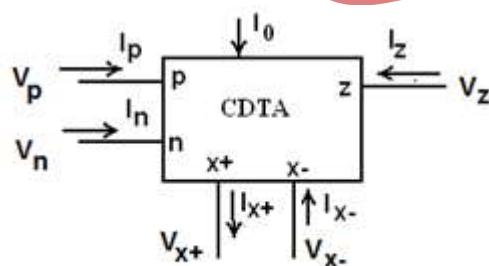


Fig. 1 Circuit symbol for CDTA

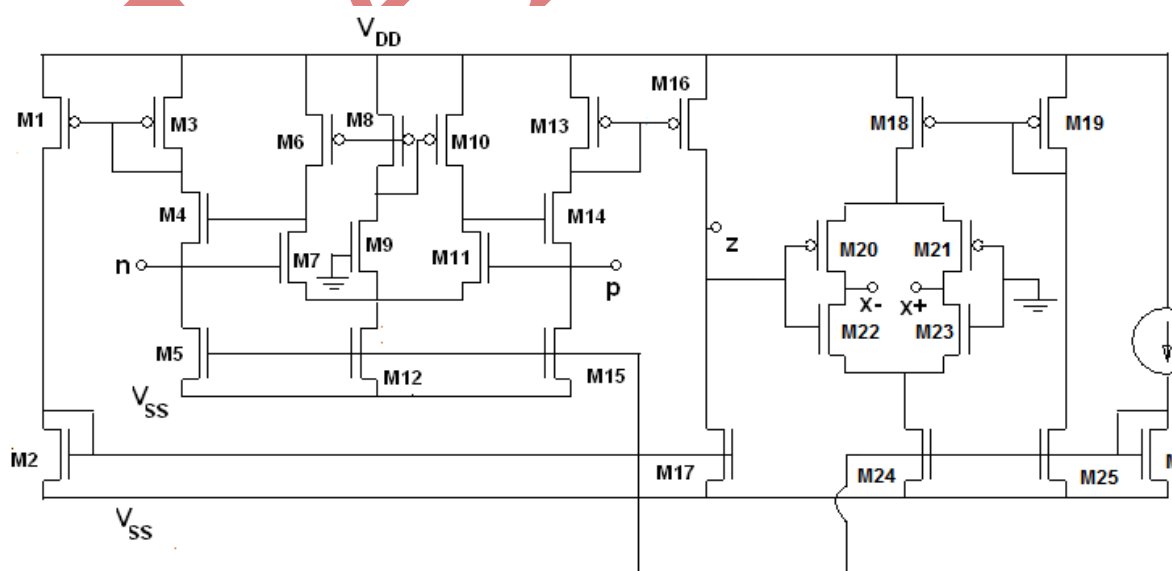


Fig. 2 CMOS CDTA implementation [14]

The p and n terminals are a pair of low-impedance current inputs and auxiliary terminal z has outgoing current which is the difference of input currents. Therefore, CDTA can be thought of as a combination of a current differencing unit followed by a dual-output operational transconductance amplifier, DO-OTA.

III CDTA BASED ADC

Current mode ADC plays an important role in front end signal processing and the design of a current mode ADC using CDTA is presented in this section. A current mode comparator performs comparison between two input currents and gives binary output voltage depending on which input current is greater. Generally, one of the two input currents is a constant, known as the reference current. The output equation of current comparator can be represented as in (1) where $I_p(t)$ and $I_n(t)$ are input currents and v_{out} is the output voltage.

$$v_{out}(t) = \begin{cases} 1, & \text{for } I_p(t) > I_n(t) \\ 0, & \text{for } I_n(t) > I_p(t) \end{cases} \quad (1)$$

The input current and the reference current is supplied to p and n terminals of CDTA. The z terminal is left open therefore the voltage at X+ and X- terminals i.e. V_{X+} and V_{X-} saturate at V_{DD} or V_{SS} [7]. The output of the CDTA is taken from X+ terminal and two cascaded CMOS inverters are used to bring the output voltage to 0- V_{DD} range.

The general schematic of a 2-bit current mode flash ADC is shown in Fig. 3. A flash ADC has the highest speed of any type of ADC [15]. It uses one comparator per quantization level and the $2^N - 1$ reference currents are generated and fed to each comparator. The input signal is compared to the reference level and the output of each comparator is a binary 1 or 0. The output of all the comparators together forms a thermometer code which is converted into binary code using a code converter circuit. The thermometer to binary encoder was designed using transmission gates and the implementation is shown in Fig. 4 with thermometer code (C1, C2 and C3) and the binary output (B0 and B1). The Boolean expression for the thermometer to binary code conversion is represented by (2) and (3).

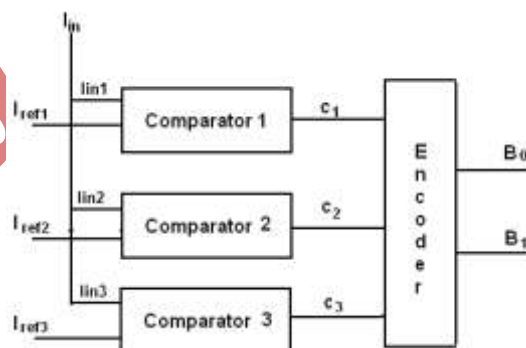


Fig. 3 2 bit Flash ADC

$$B_0 = C_1 * C_2 + C_3 * \overline{C_2} \quad (2)$$

$$B_1 = C_2 \quad (3)$$

The ADC was designed to work in the current range 0-40 μ A with a step size of 10 μ A. The reference currents I_{ref1} , I_{ref2} , I_{ref3} were accordingly set at 5 μ A, 15 μ A and 25 μ A respectively. The input current was mirrored into I_{in1} , I_{in2} and I_{in3} using a regulated cascode current mirror. The performance of the ADC is generally characterized by the parameters resolution, sampling rate, INL, DNL, offset and gain error. These parameters were measured through simulations and are presented in the simulation section.

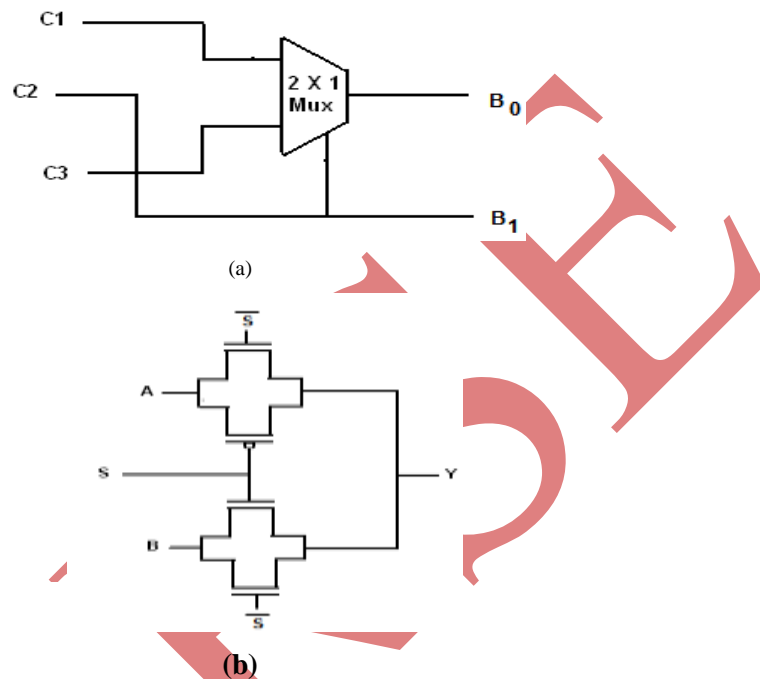


Fig. 4 (a) Encoder using multiplexer (b) TG based multiplexer implementation

IV SIMULATION RESULTS

The 2-bit flash current mode ADC using CDTA was implemented in 0.35 μ m CMOS technology in ORCAD PSIPCE and the corresponding transistor widths are reported in Table I. All the transistor lengths were set at 0.7 μ m. The simulation conditions are reported in Table II.

TABLE I. TRANSISTOR DIMENSIONS FOR CMOS CDTA-ADC

Transistor No.	W(μ m)
M1	9.8
M2-3, M13, M16-17	10.5
M4, M14	42
M5, M12, M15	35
M6, M8, M10, M21	28
M7, M9, M11	70
M18, M24-25	56
M19	58.8
M20	28.7
M22-23	16.1
M26	7

TABLE II. SIMULATION CONDITION FOR CDTA BASED CURRENT MODE ADC

Temperature	27°C
Technology	0.35µm CMOS
Power Supply	1.8 V
Iref _{i=1,2,3}	5µA, 15µA, 25µA

The CDTA based ADC was fed with input current in the range of 0-40µA and DC analysis was carried out. The corresponding output for is shown in Fig. 5. The input currents at which the ADC output transitions occurred were noted and these were used to construct the actual ADC transfer characteristic. This is shown in Fig. 6 along with the ideal ADC transfer characteristic and it is seen that the ADC doesn't suffer from missing codes. The DNL and the INL were calculated from Fig. 6 and are plotted in Fig. 7 and Fig. 8 respectively. The DNL is -0.45LSB and the INL is -0.000225LSB and both are much lower than the maximum value of half of least significant bit (LSB), with $LSB/2 = 5 \mu A$. The offset and the gain error were calculated as 0.5µA and 0.98 respectively. To characterize the speed of the CDTA based ADC, transient analysis was performed by feeding input pulse of 0-40 µA amplitude and frequency 500 KHz. The maximum delay under the above input conditions was found to be 81.332ns. The ADC was also subjected to sine input of frequency 6 MHz and it showed correct output as demonstrated by Fig. 9.

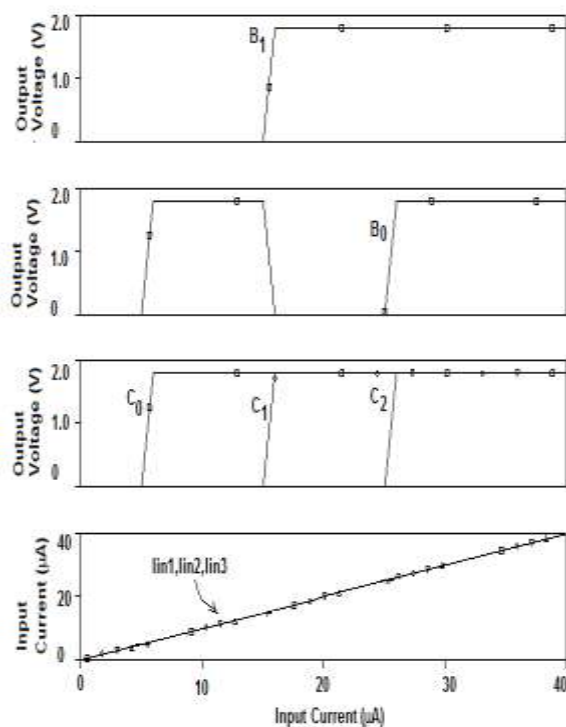


Fig. 5 ADC output for ramp input

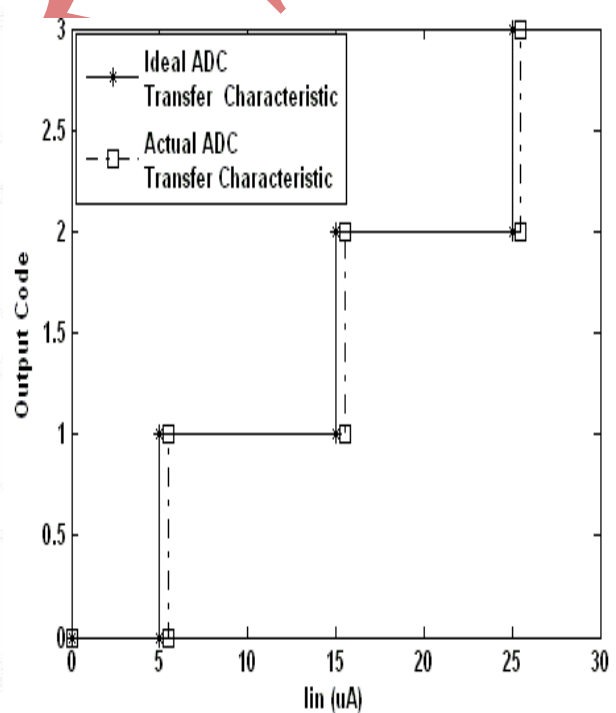


Fig. 6. Ideal and simulated ADC characteristics

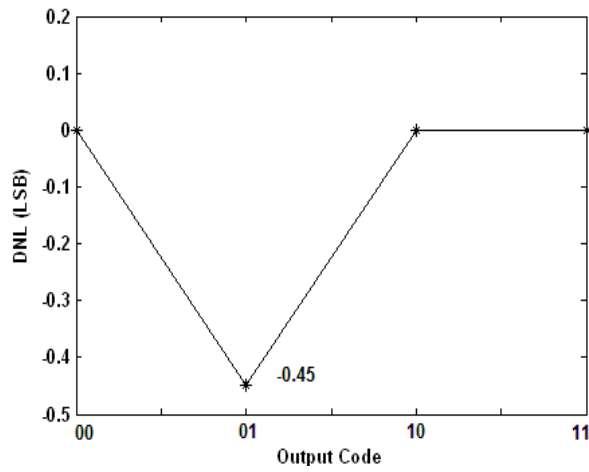


Fig. 7 DNL versus Output Code

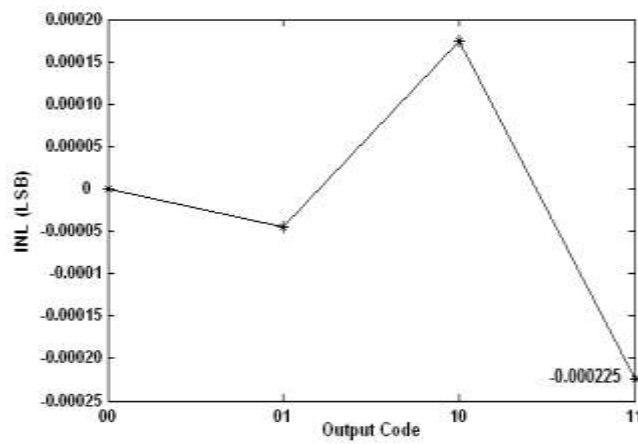


Fig. 8 INL versus Output Code

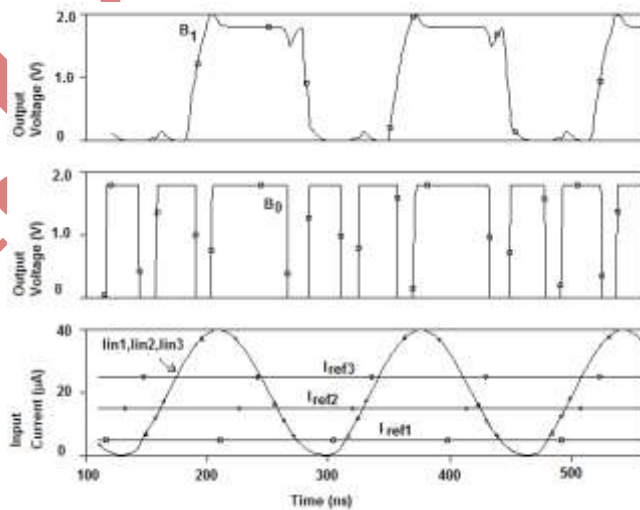


Fig. 9 ADC Output For Input Sine of Frequency 6 Mhz

V CONCLUSION

In this paper, a newly introduced active building block the current differencing transconductance amplifier (CDTA) is used for implementation of a current mode ADC. This application of CDTA has not yet been enumerated elsewhere and the results from the simulation section are promising. The INL and DNL of the CDTA based ADC is much lower than the maximum value of half of least significant bit (LSB). It also shows a delay of around 80ns at an input pulse of 500 KHz.

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