SIMULATED DESIGN OF 5 STAGE CMOS RING OSCILLATOR FOR HIGH SPEED TRANSMITTER AT 5 GHz

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ABSTRACT

This paper represents a 5 stage voltage-controlled ring oscillator at 5 GHz for "High Speed Serial Link". The circuit is implemented using 180 nm CMOS technology in CADENCE VIRTUOSO with 3.3V supply. The high Q low-pass filter is used to make the signal free from noise and jitter. The circuit dissipates 8.202 milliwatt of power in the frequency range of 1Hz-5GHz. This high speed technology shows greater reliability and greater efficiency as compared to giga-bit and Ethernet standard but due to this high speed , inter-symbol interference comes into existence in a channel.

Keywords

Inter-symbol interference, jitter, phase-locked loop,voltage-controlled oscillator, voltage-stabilizer.

I. INTRODUCTION

The long-way path from high power technology to low-power technology begins with the advancement of scaling technology, increase of resistance R and obviously high-speed data-rate. The serial-link structure performed at high speed offers significant flexibility both in case of fibre-channel and giga-bit Ethernet standard. The interfered signals in a channel form the shape of an eye.

The shared bus model of high-speed signaling system is typically based on integrated system technology. These shared buses occupy greater area and dissipates a large amount of power. The shared bus model is widely used in 100-200 Mbps multiprocessor systems and in the field of network switching circuits ([1], [2], [3]) for short range distances. On the other hand, point to point model has been implemented for multi-gbps application through a distance of several kilometers and easily avoid the disadvantage of bandwidth limitation.

The voltage-controlled oscillator lies in the heart of the serial link system. The key role of VCO in a RF transmitter is to control the frequency. In the field of "Very Large Scale Integration" , the CMOS ring structure of VCO is more preferable than LC tuned oscillator because of its higher level of integration [5]. As gallium arsenide (GaAs) offers higher intrinsic device speed as compared to silicon or germanium, it is most widely used for CMOS structure in VCO.

This paper is organized as follows: High speed serial link background is presented in section II, circuit design in section III , results are described in section IV and conclusion is in section V.

II. SERIAL-LINK AT HIGH FREQUENCY

The designers use 200 milli-volt peak to peak differential swing for the general serial-link structures and because of these low swings only, a small amount of stray signal can also create a significant problem. As a result, the effect of noise in a transmission line is much more-effective when the data-rate becomes 10 Gbps or the evenly placed signal attains a frequency of 5GHz.

The high Q low-pass filter is used in a phase-locked loop of high speed transceiver. The filter circuit can also be implemented using an injection-locked oscillator (ILO) circuit but the behavior of a first order PLL circuit closely resembles the closed loop circuit of ILO [6].

The working principle of ILO depends on the local oscillation frequency. If the frequency difference of the injection-locked oscillator and local oscillation will be very small, then ILO will automatically lock the phase of the signal which is injected ([7], [8]).

According to the loop dynamics of phase-locked loop, phase-locked condition is generally required to inhibit the change of phase. Phase frequency detector is used in a phase-locked loop because the VCO acts as a voltage-stabilizer by inhibiting its change of phase [9].

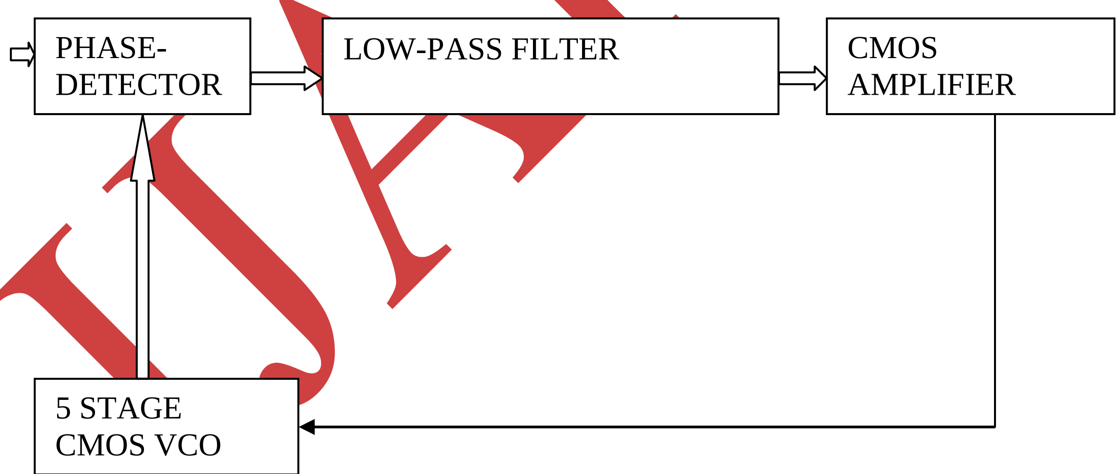

Fig 1 Basic Block Diagram of Phased-Locked Loop

III. CIRCUIT DESIGN

The main design while designing RF transmitter is its stability, linearity, power transfer and impedance matching. Our work uses a 5 stage voltage-controlled ring oscillator, originally proposed by Tibor Grasser to generate frequency in 10 evenly spaced phases.

The low-pass filter acts as a filtrator of noise and the CMOS amplifier amplifies the signal which is again fed into VCO. The output of VCO is used to compare the phase difference in between input signal and output of VCO by phase-detector. This will simply measure the phase-shift in case of a RF transmitter.

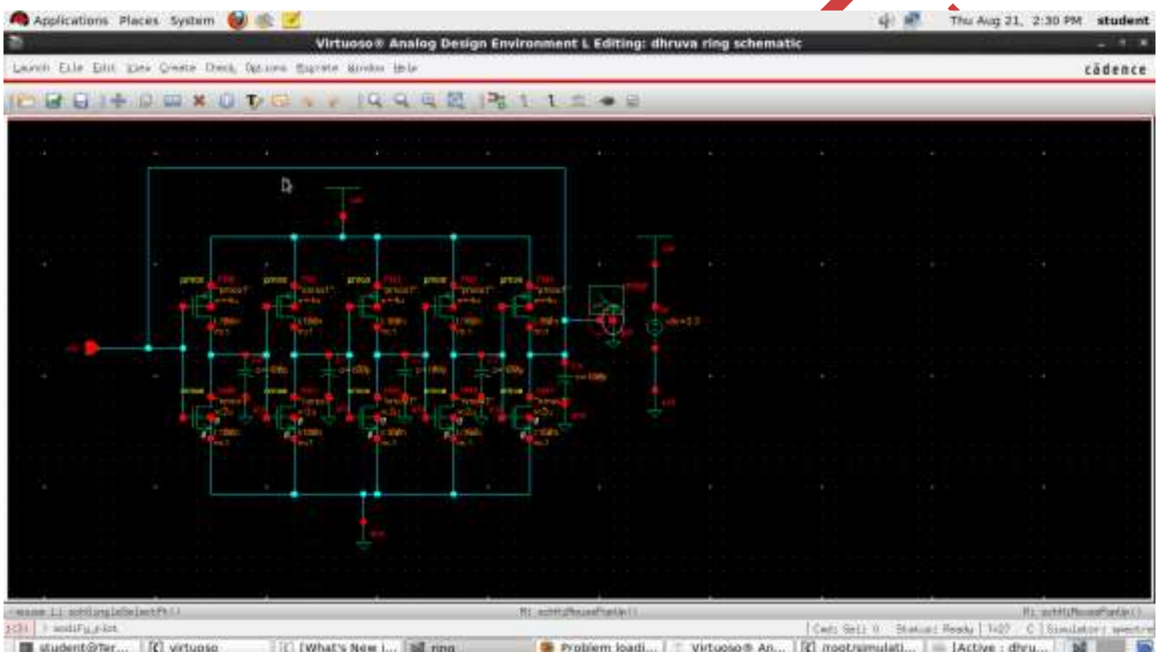

Fig 2 Circuit diagram of 5 stage CMOS VCO

The phase-locked loop generally acts as an integrator and the charge pump converts currents into voltage. For an n stage ring oscillator, the oscillation frequency [10] will be,

$f = 1/n(\tau_{rise}+\tau_{fall})$……………………………………………………………………………….(1)

As oscillation frequency, f=1/T, then average power [11] will be,

P (avg)=[(Vsupply)^2*Cload]/T…………………………………………………………………………..(2)

IV. RESULTS AND DISCUSSION

The operation of VCO is tested in the frequency range of 1Hz-5GHz. The major issue of circuit design is low power dissipation. Our circuit dissipates 8.202 milliwatt of power in the frequency range of 1Hz-5GHz.

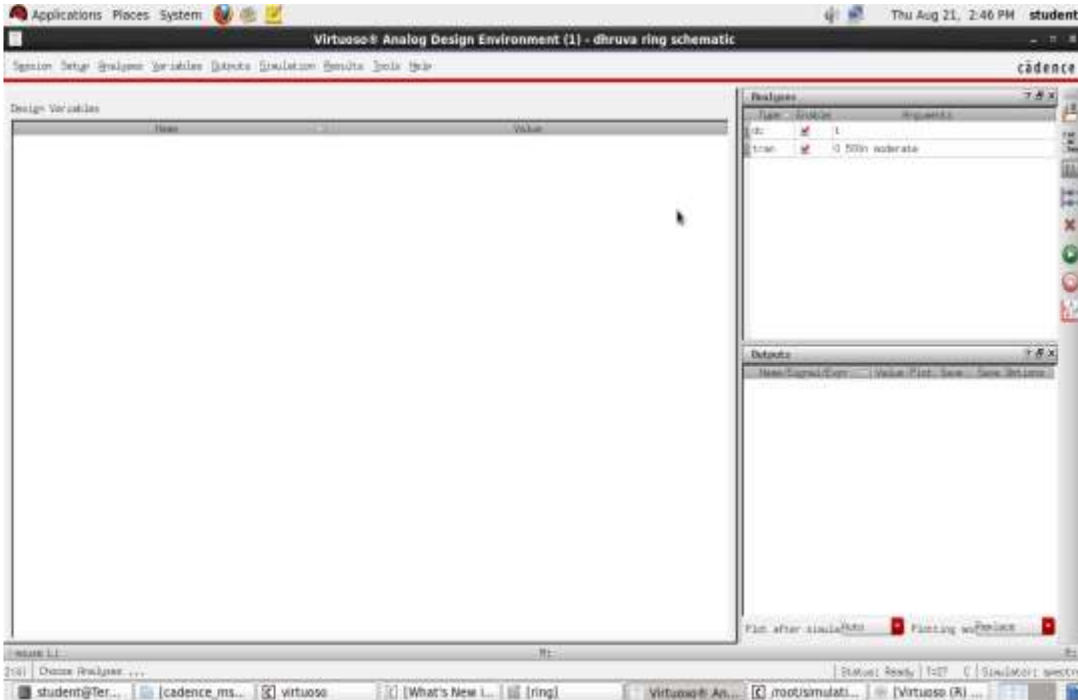

Fig 3 Virtuoso Analog Design Environment While Simulating Average Power

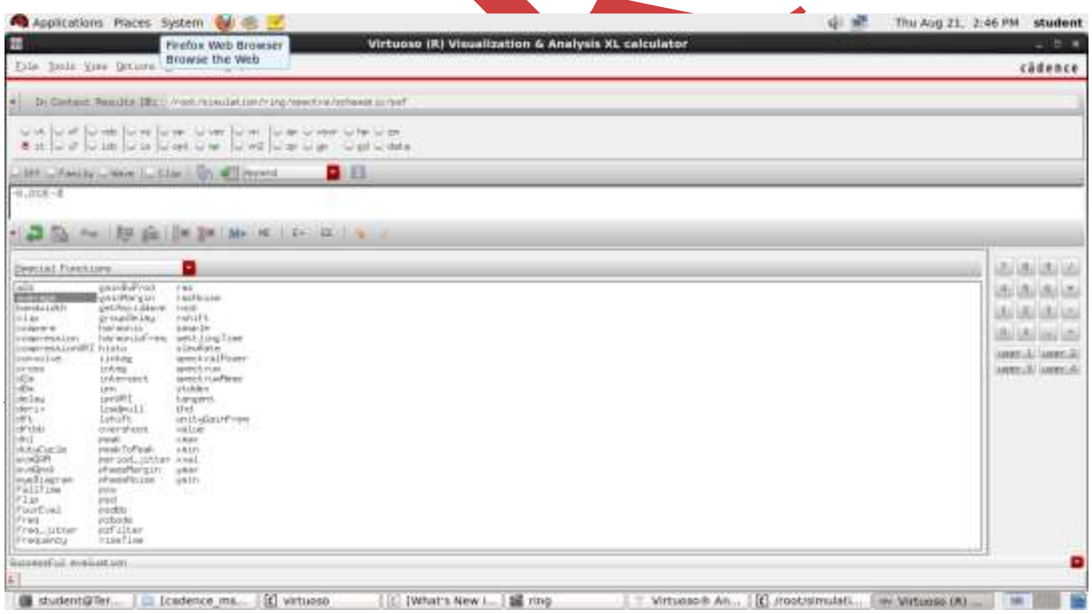

Fig 4 Simulation result of average power of 5 stage CMOS ring oscillator in the frequency range of 1Hz-5GHz with 3.3V supply

TABLE1

Comparison of performance of various types of oscillators in terms of power

Reference	Type/Technology	Frequency(GHz)	Supply(V)	Power(milliwatt)
[12]	Vacker VCO/180nm	4.85-4.93	1.8	13.5
[13]	Armstrong VCO/180nm	4.96-5.34	1.8	3.9
[14]	Colpitt's VCO/180nm	4.9-5.26	1.8	6.4
[15]	Ring VCO/180nm	5.16-5.93	1.8	27
[16]	Hartley VCO/180nm	4.02-4.5	1.8	6.75
Our work	5 stage CMOS VCO/180nm	1Hz-5GHz	3.3	8.202

Table1 clearly proves that our work constitutes of a better and easier VCO structure as compared to others and dissipates 8.202 milliwatt of power.

V. CONCLUSION

The major issue to design a transceiver is to maintain the integrity of the signal along the channel. Our result proved that the 5 stage CMOS ring oscillator idea which was first proposed by Tibor Grasser has designed successfully and dissipating 8.202 milliwatt of power in the frequency range of 1Hz-5GHz.

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