DIAGNOSIS OF FAULT IN TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS USING MULTIPLEXER CONSERVATIVE QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1s, and all 0s. The designs of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops are presented. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the need for any type of scan-path access to internal memory cells. The reversible design of the DET flip-flop is proposed for the first time in the literature. The application of the proposed approach toward 100% fault coverage for single missing or additional cell defect in the quantum dot cellular automata (QCA) layout of the Fredkin gate. A new conservative logic gate called multiplexer conservative QCA gate (MX-cqca) that is not reversible in nature but has similar properties as the Fredkin gate of working as 2:1 multiplexer. The proposed MX-cqca gate surpasses the Fredkin gate in terms of complexity (the number of majority voters), speed, and area.

Keywords–DET,QCA,MX-cqca.

I INTRODUCTION

Reversible logic has promising applications in emerging nanotechnologies, such as quantum computing, quantum dot cellular automata and optical computing, etc. Faults in reversible logic circuits that result in multibit error at the outputs are very tough to detect, and thus in literature, researchers have only addressed the problem of online testing of faults that result single bit error at the outputs based on parity preserving logic. In this work, we propose a methodology for the concurrent error detection in reversible logic circuits to detect faults that can result in multi bit

error at the outputs. The methodology is based on the inverse property of reversible logic and is termed as inverse and compare method. By using the inverse property of reversible logic, all the inputs can be regenerated at the outputs.

Thus, by comparing the original inputs with the regenerated inputs, the faults in reversible circuits can be detected. Minimizing the garbage outputs is one of the main goals in reversible logic design and synthesis. The proposed methodology results in garbage less reversible circuits. A design of reversible full adder that can be concurrently tested for multi bit error at the outputs is illustrated as the application of the proposed scheme. The application of the scheme of concurrent error detection towards fault detection in quantum dot cellular automata QCA emerging nanotechnology. Reversible logic has applications in quantum computing, low power CMOS, nanotechnology, optical computing, and DNA computing. The most common reversible gates are the Toffoli gate and the Fredkin gate. The synthesis algorithm has a cascade of Toffoli and Fredkin gates with no backtracking and minimal look ahead. Transformations that reduce the size of the circuit is applied. Transformations are accomplished via template matching. The basis for a template is a network with m gates that realizes the identity function. If a sequence in the network to be synthesized matches more than half of a template, then a transformation that reduces the gate count can be applied. In this paper we show that Toffoli and Fredkin gates behave in a similar manner. Therefore, some gates in the templates may not need to be specified they can match a Toffoli or a Fredkin gate.

II. LITERATURE REVIEW

2.1. Reversible Logic-Based Concurrently Testable Latches for Molecular QCA.

Nanotechnologies, including molecular quantum dot cellular automata (QCA), are susceptible to high error rates. In this paper, we present the design of concurrently testable latches (D latch, T latch, JK latch, and SR latch), which are based on reversible conservative logic for molecular QCA. Conservative reversible circuits are a specific type of reversible circuits, in which there would be an equal number of 1's in the outputs as there would be on the inputs, in addition to one-to-one mapping. Thus, conservative logic is parity-preserving, i.e., the parity of the input vectors is equal to that of the output vectors. The fault patterns in the conservative reversible Fredkin gate due to a single missing/additional cell defect in molecular QCA.

If there is a fault in the molecular QCA implementation of Fredkin gate, there is a parity mismatch between the inputs and the outputs, otherwise the inputs parity is the same as outputs parity. Any permanent or transient fault in molecular QCA can be concurrently detected if implemented with the conservative Fredkin gate. The design of QCA layouts and the verification of the latch designs using the QCA Designer and the HDLQ tool are presented. The use of conservative reversible logic based on Fredkin gate to design concurrently testable sequential circuits for molecular QCA. The proposed concurrent testing methodology is based on parity-preserving property of Fredkin gate, and is beneficial for both permanent and transient faults that results in parity mismatch between inputs and outputs.

2.2. Constructing Online Testable Circuits Using Reversible Logic

With the advent of nanometer technology, circuits are more prone to transient faults that can occur during its operation. Of the different types of transient faults reported in the literature, the single-event upset (SEU) is prominent. Traditional techniques such as triple-modular redundancy (TMR) consume large area and power. Reversible logic has been gaining interest in the recent past due to its less heat dissipation characteristics. This paper proposes the following: (1) a novel universal reversible logic gate (URG) and a set of basic sequential elements that could be used for building reversible sequential circuits, with 25% less garbage than the best reported in the literature; (2) a reversible gate that can mimic the functionality of a lookup table (LUT) that can be used to construct a reversible field-programmable gate array (FPGA); and (3) automatic conversion of any given reversible circuit into an online testable circuit that can detectonline any single-bit errors, including soft errors in the logic blocks, using theoretically proved minimum garbage, which is significantly lesser than the best reported in the literature. This paper has proposed several reversible circuits for realizing both combinational and sequential elements of a given digital circuit.

A URG, which is shown to be advantageous for synthesizing multivalued reversible logic, was presented. This paper has also proposed a reversible gate that can mimic the functionality of a two-input LUT, thus enabling the memory less realization of LUTs. This can be used as a programmable logic block in modern field-programmable gate array architectures. This paper has presented efficient realizations of reversible sequential elements. The proposed designs lead to a 25% reduction in garbage and a lesser number of 3 × 3 reversible gates when compared with the best reported in the literature. This paper has also proposed a methodology that automatically converts any circuit into an online testable reversible circuit with theoretically proved minimum garbage. The resultant testable circuit can detect online any singlebit errors in the logic blocks. An important advantage of the technique is that the design of a given reversible circuit need not be changed for the purpose of adding testability feature to it. This paper has discussed the construction of hierarchical multi modular online testable reversible circuits.

III. PROPOSED METHOD

3.1 Reversible Logic

Reversible logic are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. This paper proposes an improved design of a adder using reversible logic gates. Adders are very essential for the construction of various computational units of a quantum computer. The quantum cost of a reversible logic circuit can be minimized by reducing the number of reversible logic gates. Reversible logic is considered as the emerging technologies in the field of optical computing, low power design and nano electronics. It has been proved that reversible logic ideally dissipates zero power. In processing systems, adder plays an important role. Hence in this work, we proposed an efficient full adder design using reversible logic. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Hence in this work, we are going to propose an efficient adder design

using carry skip adder and carry select adder and implemented it in reversible logic. The design to be proposed gives minimum number of gates, garbage outputs and quantum cost there by reducing the power consumption, area, delay.

3.2 Fredkin Gate

The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

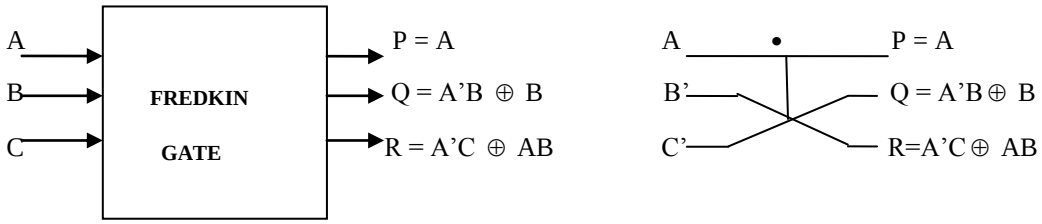

Fig. 3.1 Fredkin Gate

Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors.Reversible logic supports the process of running the system both forward and backward. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

Table 3.1 Truth table of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	1

3.3 Design of Testable Reversible Latches

In the proposed work (E) to the clock and is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q^+ = D. While, when E = 0 the latch maintains its

previous state, that is $Q^+ = Q$. The reversible Fredkin gate has two of its outputs working as 2:1 MUXES, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F). Figure. 3.2 shows the realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault. In this paper, we propose to cascade another Fredkin gate to output Q as shown in Figure. 3.2. The design has two control signals, C1 and C2. The design can work in two modes.The normal mode is shown in Figure. 3.2 in which we will have C1C2 = 01 and we will have the design working as a D latch without any fan-out problem. Test Mode (Disrupt the Feedback): In test mode, when C1C2 = 00 as shown in Figure.3.2 it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected. When C1C2 = 11 as shown in Figure.3.2, the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault. It can seen from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fan-out. Thus, our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

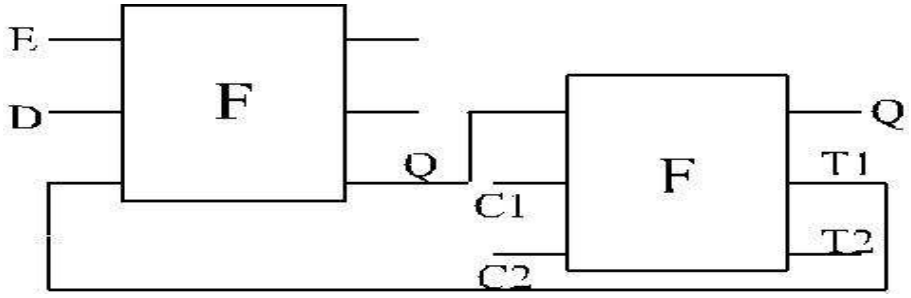

Fig. 3.2. Fredkin Gate D Latch with control signals C1 and C2.

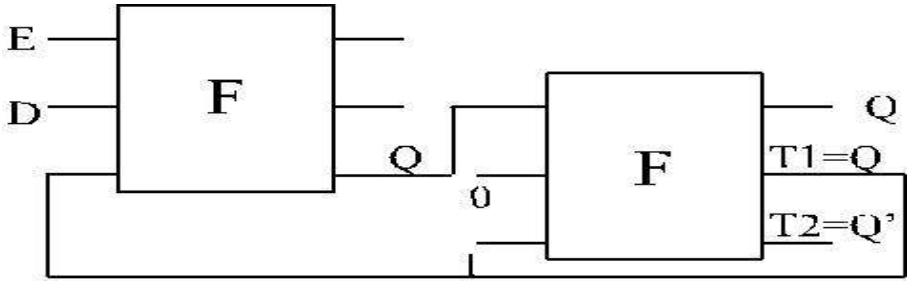

Fig. 3.3. Fredkin Gate D Latch in normal mode: C1=0 and C2=1

3.4 Design of Testable Negative Enable Reversible D Latch

A negative enable reversible D latch will pass the input D to the output Q when E = 0; otherwise maintains the same state. The characteristic equation of the negative enable D latch is

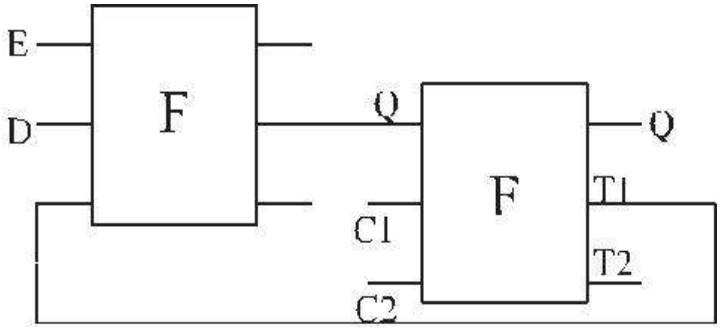

Fig. 3.4. Fredkin Gate based Negative Enable Testable D Latch

The other type of master-slave flip-flops, such as the testable master-slave T flip-flop, testable master-slave JK flip-flop, and testable master-slave SR flip-flop can be designed similarly in which master is designed using the positive enable corresponding latch, while the slave is designed using the negative enable Fredkin gate-based D latch.

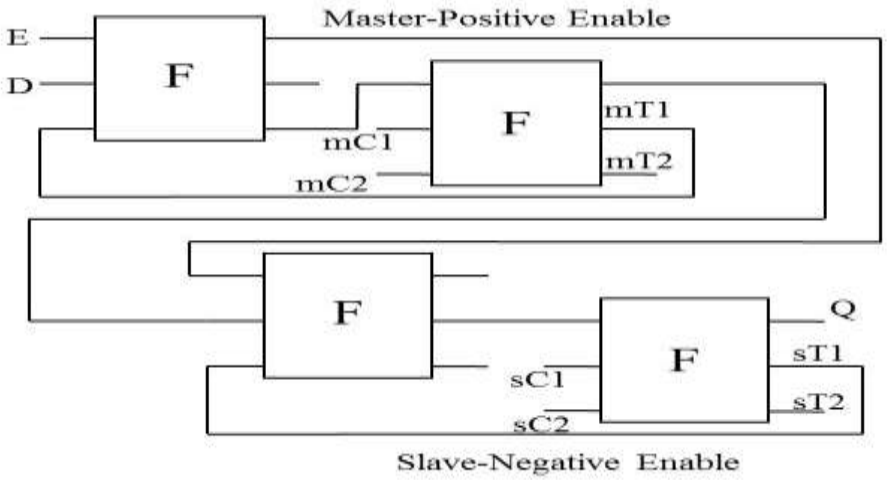

Fig. 3.5. Fredkin Gate based Testable Reversible Master-slave D Flip-flop

To make the design testable with all 0s input vectors for any stuck-at-1 fault, the values of the controls signals will be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0. This will make the outputs mT1 and sT1 as 0, which results in breaking the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault. To make the design testable with all 0s input vectors for any stuck-at-1 fault, the values of the controls signals will be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0. This will make the outputs mT1 and sT1 as 0, which results in breaking the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault. To make the design testable with all 1s input vectors for any stuck-at-0 fault, the values of the control signals will be mC1 = 1 mC2 = 1, sC1 = 1, and sC2 = 1. This will result in outputs mT1 and sT1 having a value of 1, breaking the feedback and resulting in the design testable with all 1s input vectors for any stuck-at-0 fault.

3.5 Design of Testable Reversible DET Flip-Flops

The DET flip-flop is a computing circuit that samples and stores the input data at both the edges, that is at both the rising and the falling edge of the clock. The master-slave strategy is the most popular way of designing the flip flop. In the proposed work, E refers to the clock and is used interchangeably in place of clock. In the negative edge triggered master-slave flip-flop when E = 1 (the clock is high), the master latch passes the input data while the slave latch maintains the previous state. When E = 0 (the clock is low), the master latch is in the storage state while the slave latch passes the output of the master latch to its output. Thus, the flip-flop does not sample the data at both the clock levels and waits for the next rising edge of the clock to latch the data at the master latch.

In order to overcome the above problem, researchers have introduced the concept of DET flip-flops, which sample the data at both the edges. Thus, DET flip-flops can receive and sample two data values in a clock period thus frequency of the clock can be reduced to half of the master-slave flip flop while maintaining the same data rate. The half frequency operations make the DET flip flops very much beneficial for low power computing as frequency is proportional to power consumption in a circuit. The DET flip-flop is designed by connecting the two latches, viz., the positive enable and the negative enable in parallel rather than in series. The 2:1 MUX at the output transfer the output from one of these latches which is in the storage state (is holding its previous state).

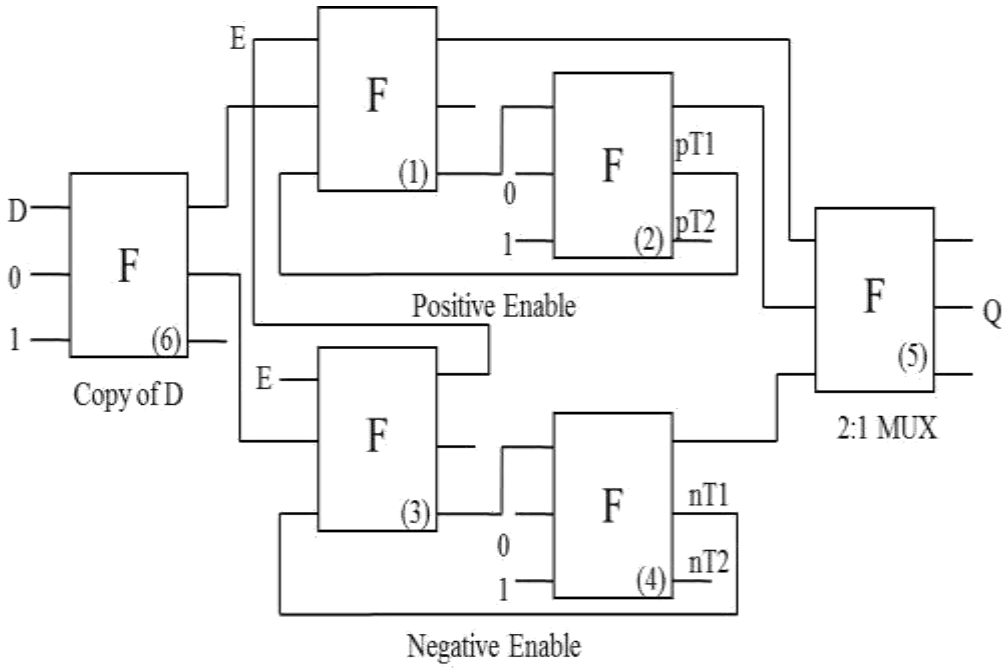

Fig. 3.6. Fredkin Gate based DET Flip-flop normal mode

Normal Mode: The normal mode of the DET flip-flop is illustrated in Figure. 4.9 in which the pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The pC1 = 0, pC2 = 1 help in copying the output of the positive enable D latch thus avoiding the FO while the nC1 = 0 and nC2 = 1 help in copying the output of the negative enable D latch thus avoiding the FO.

IV. SIMULATION AND ANALYSIS

4.1 Simulation Environment

Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing.

4.2 Output Waveform of Fredkin Gate

The Figure 4.2 shows the waveform of fredkin gate for the input ain, bin, cin and the respective outputs p0, q0,r0.

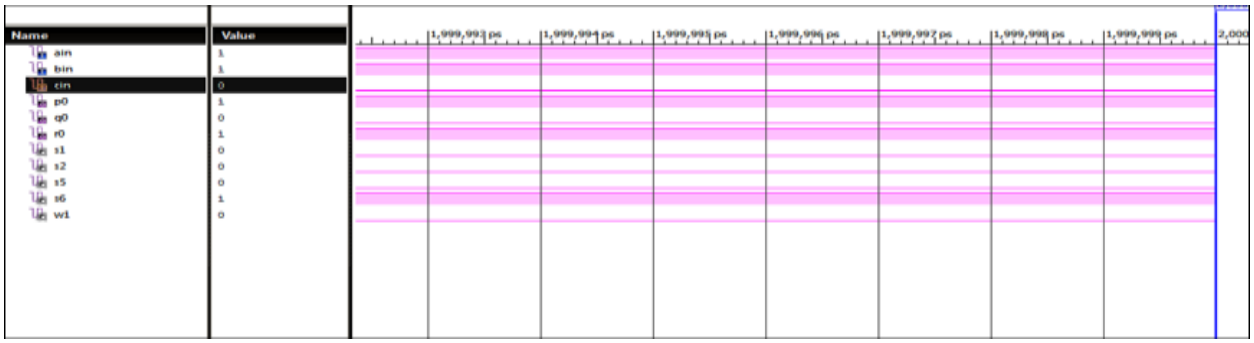

Fig. 4.2 Input Output Waveform of Fredkin gate

4.3 Output Waveform of Fredkin Gate Based Testable Reversible Master-Slave D Flipflop

The Figure 4.3 shows the output waveform of fredkin gate based testable reversible master-slave d flipflop for the inputs e,d,mc1,mc2,sc1,sc2 and the respective output mt2,st2 .

Fig. 4.3 Input Output Waveform of Fredkin gate based Testable Reversible Master-slave D Flipflop

4.4 Output Waveform of Fredkin Gate Based Testable Reversible Master-Slave D Flipflop for Stuck-At-1 Fault

The Figure 4.4 shows the output waveform of fredkin gate based testable reversible master-slave d flipflop for the inputs e,d,mc1,mc2,sc1,sc2 and the respective output mt2,st2 .

Fig. 4.4 Input Output Waveform of Fredkin gate based Testable Reversible Master-slave D Flipflop for stuck-at-1 fault

4.5 Output Waveform of Fredkin Gate Based Det Flipflop

The Figure 4.5 shows the output waveform of fredkin gate based DET flipflop for the inputs e,d,dc1,dc2,pc1,pc2,nc1,nc2 and the respective output pt2,nt2 .

Fig. 4.5 Input Output Waveform of Fredkin gate based DET Flipflop

IV. CONCLUSION

The proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed sequential circuits based on conservative logic gates outperform the sequential circuit implemented in classical gates in terms of testability. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In future this limitation has to be over come.

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