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DESIGN OF MULTIPLIER USING GDI TECHNIQUE

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ABSTRACT

Multiplier is the most commonly used circuit in digital devices. Multiplication is one of the fundamental functions that used in digital signal processing. Mostly high performance DSP systems that rely on hardware multiplication to achieve high data throughput. There are many types of multipliers available depending upon the application in which they are used. We propose a Gate Diffusion Input (GDI) based cell design for 4-bit array multiplier, which is found to be much more power efficient in comparison with existing multiplier design. It ultimately reduces the Power consumption. Here the 4-bit multipliers based on GDI cells are designed using EDA Tanner and simulations are based on 180nm CMOS technology. The transistor count is reduced to 136 when compared with CPL Multiplier which requires 200 transistors.

Keywords : CPL, DSP, GDI ,Low power ,Multiplier

I INTRODUCTION

The integration of a large number of functions on a single chip usually provides

- Less area/ volume and hence compactness
- Less power consumption
- Less testing requirements at system level
- Cost effective

Multiplier is the most commonly used circuit in the digital devices. Designing multiplier circuit efficiently we can reduce the power consumption of the circuit. Various blocks of multiplier are AND gate, Half Adder and full adder

1.1 Adder

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Adders serves as a main building block for synthesis and all other arithmetic operations. The efficient implementation of an arithmetic unit and the binary adder structures become a very critical hardware unit. A full adder shown in Figure 1 is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, both of which are binary digits

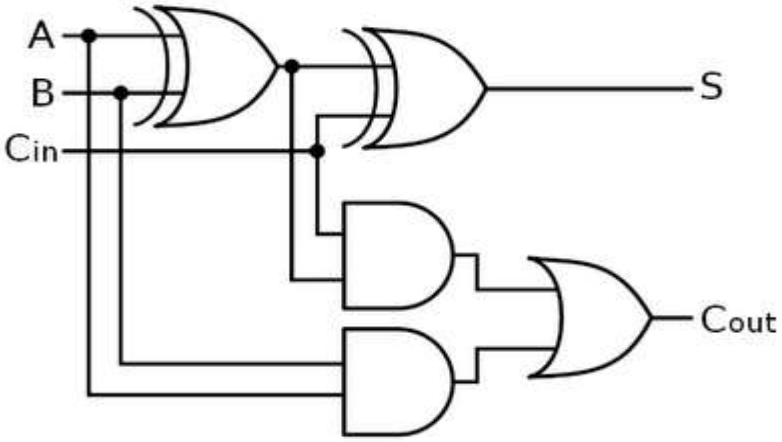

Figure 1. Full Adder Circuit

1.2 Multipliers

Multiplication is an operation that occurs frequently in digital signal processing and many other applications. However, multipliers occupy a much larger area and incur much longer delays than adders. Therefore it is imperative that special techniques be used to speed up the calculation of the product while maintaining a reasonable area. A multiplier can be divided into three stages: first one is Partial products generation stage, second is partial products addition stage, and the final addition stage. In the first stage, the multiplier and the multiplicand are multiplied bit by bit to generate the partial products. The second stage is more complicated and it determines the speed of the overall multiplier. The multipliers play a major role in arithmetic operations in digital signal processing (DSP) applications. The present development in processor designs aim at design of low power multiplier. So, the need for low power multipliers has increased. Generally the computational performance of DSP processors is affected by its multipliers performance. The multiplier structure considered for analysis is Array Multiplier. It has been implemented using different technique and their performance comparison has been made.

II EXISTING METHOD

2.1 Complementry Pass Transistor Logic

The full adder circuit designed by using complementary pass transistor logic (CPL) has swing restoration ability .It has 18 transistors based on NMOS pass-transistor network. This cause slow input capacitance and high speed operation. However it also leads to one threshold voltage (Vth) lose in the output. CPL consumes less power than standard static CMOS circuits, due to less output voltage swing that is the result of one Vth loss in the output. However it introduces noise margin and causes serious problems in cascading, especially at low voltages. Therefore,

CMOS inverters are used to restore the outputs voltage level and ensure the drivability and feeble PMOS transistors are used to minimize the static current caused by the incomplete turn-off of the PMOS in the output inverters.

The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. The main advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, and the results are in smaller number of transistors and input loads especially when NMOS network used and the pass transistor logic has an threshold voltage drop problem.

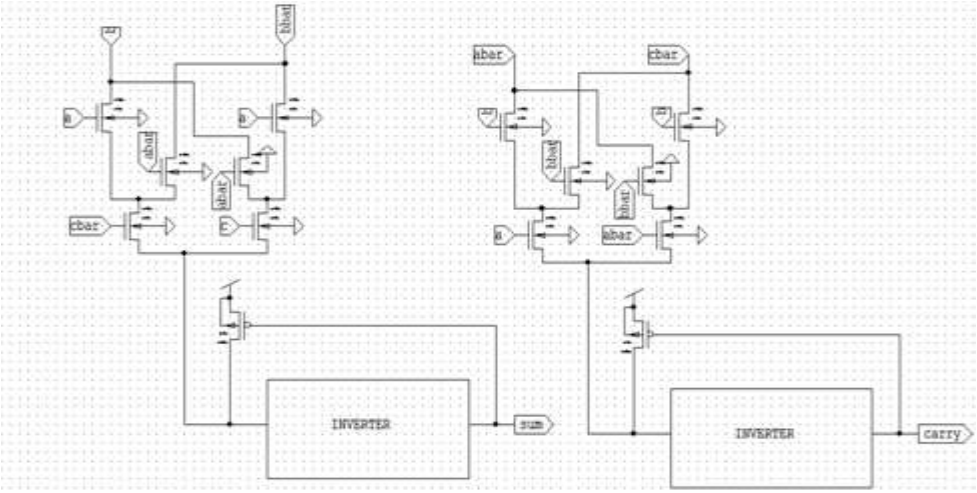

Figure 2. Schematic Of Full Adder Using CPL

The above is the schematic of Full Adder designed using CPL technology which is a part of the multiplier implemented. It requires a total of 18 transistors.

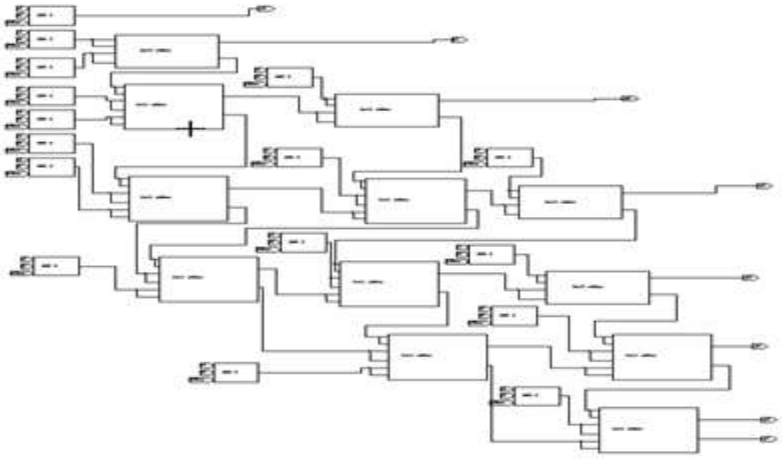

Figure 3. Schematic Of The Multiplier Using CPL

III PROPOSED METHOD

3.1 Gate Diffusion Input Technique

The GDI method is based on the use of a simple cell as shown in Figure 4. At first glance, the basic cell reminds same as the standard CMOS inverter, but there is some important differences.

1. The GDI cell contains three inputs: (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

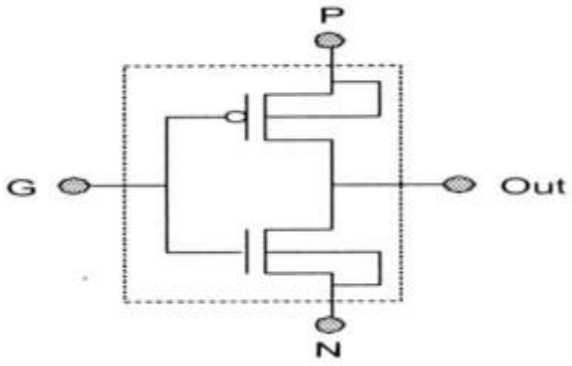

Figure 4. GDI Basic Cell

2. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies. Table 3.1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions.

3. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple process (only two transistors per function) is required for GDI technique**.**

Table 3.1 Various Logic Functions using GDI Cell

N	P	G	Out	Function
0	B	A	$\overline{A}$ B	F1
B	1	A	$\overline{A}$ +B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$ B+AC	MUX
0	1	A	$\overline{A}$	NOT

3.2 Full Adder Based On Gate Diffusion Input

A full adder is designed using two XOR Gates and a Multiplexer. Both the designs are implemented using Gate diffusion input technique.

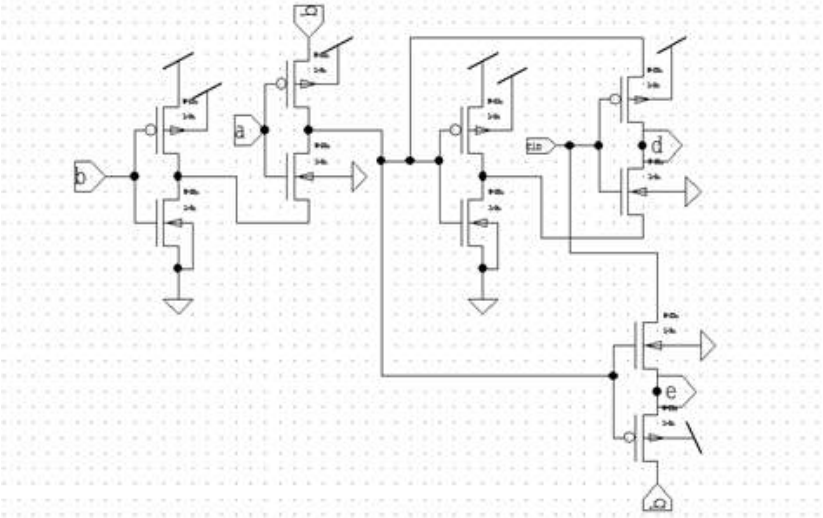

Figure 5. Schematic of Full Adder Using GDI

3.3 Multipliers to Be Implemented

The multiplier to be implemented

- ARRAY MULTIPLIER

3.3.1 Array Multiplier

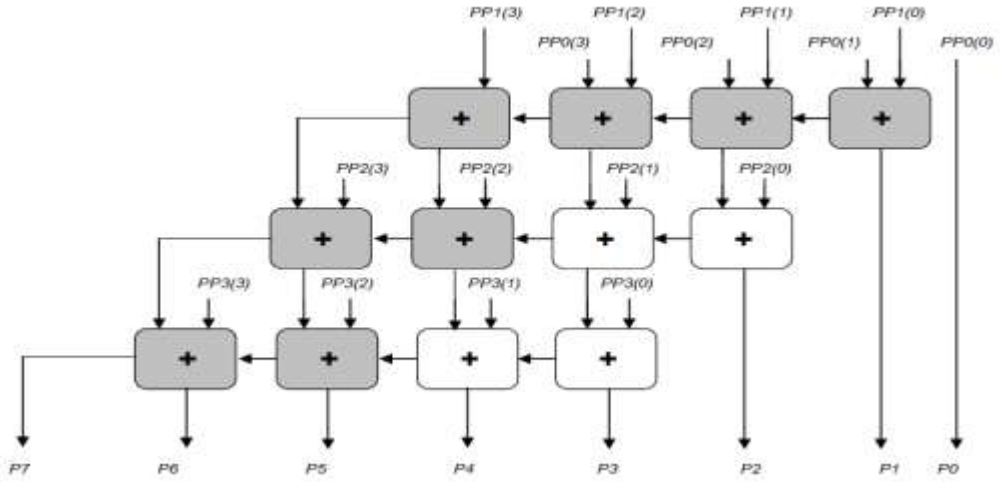

Figure 6. Array Multipliers

This is one of the simplest techniques for implementing multiplication. The idea is to add all the N partial products sequentially using N-1 adders. If we are multiplying N bit values then in effect we will need N-1 N-bit adders or N*(N-1) single adder cells. The structure of the array multiplier is shown in Figure 6**.**This figure shows that there are many identical critical paths traveling from the top right to the lower left.

Array multipliers shown in figure 6. are very slow as their critical path is very long. If we assume that the time taken to produce a sum is *klog(N)*, then the time for multiplication with an array multiplier would usually be many multiples of *klog(N)* for current practical values of N. The advantage of the array multiplier is that because of its regular structure it is easy to design and layout**.**

3.3.2 Multiplier Based On Gate Diffusion Input

A 4x4 array Multiplier is designed using 16AND gates, 8 Full Adders and 4 Half Adders.The figure shows the schematic of 4x4 array Multiplier. It requires less number of transistors and has low power consumption.

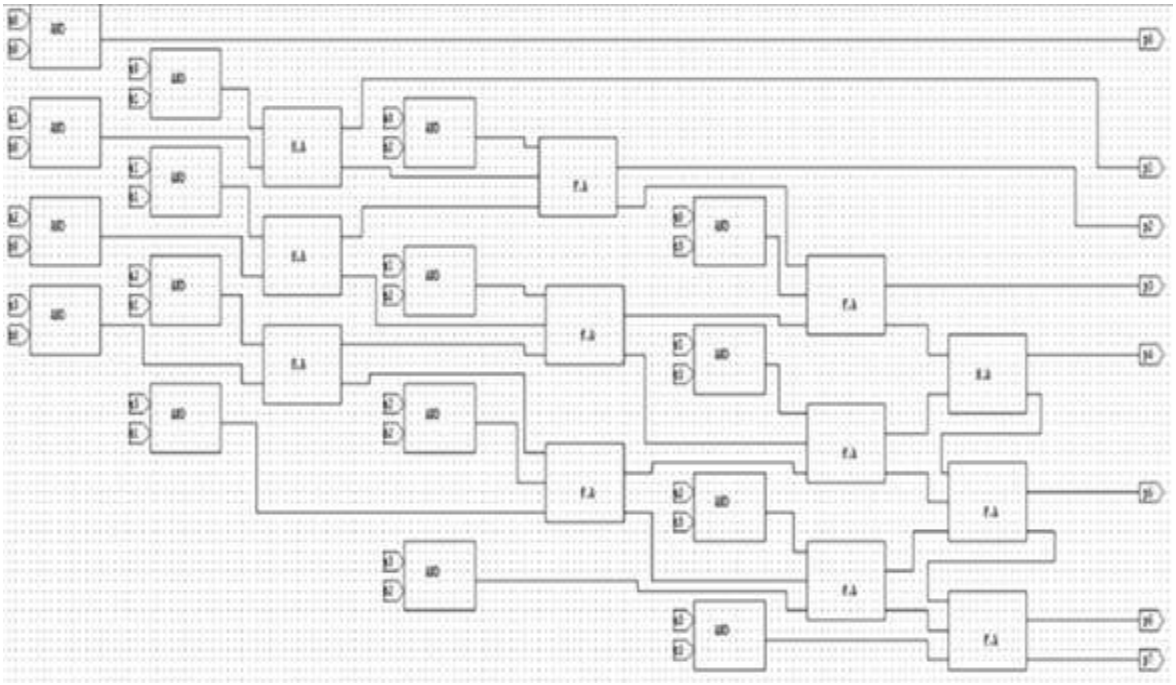

Figure 7. Schematic of Multiplier Using GDI

IV SIMULATION RESULTS

Simulation results are performed using Tanner EDA tool in 125nm technology with supply voltage of 5v. To establish an impartial testing environment each circuit have been tested on the same input patterns. Studies have been done with Complementary pass transistor and proposed GDI logic. The 4 bit array multiplier is designed and

the power consumption and number of transistors used are compared with Complementary pass transistor Logic and the proposed GDI logic.

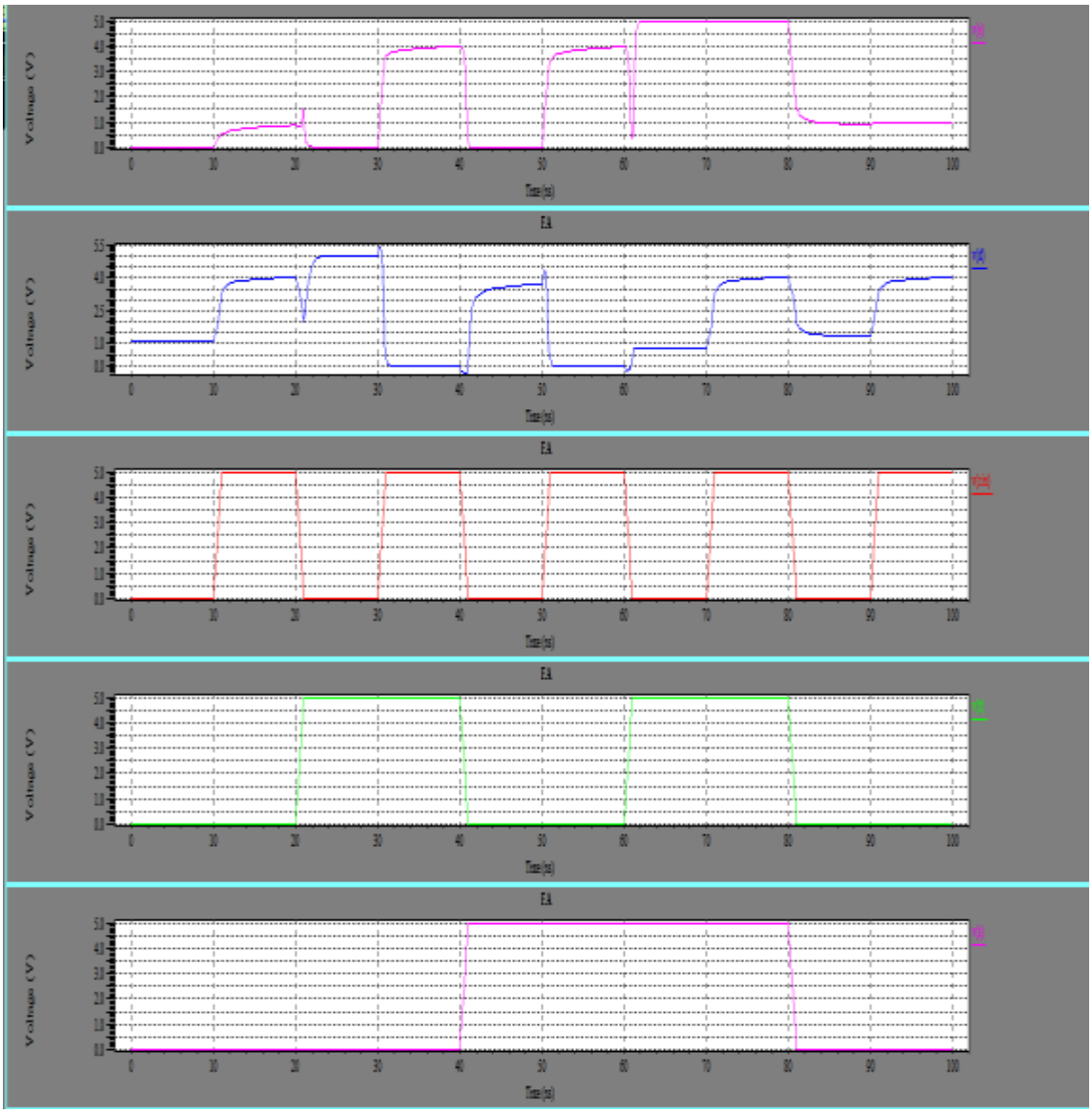

Figure 8. Waveform of Full Adder Using GDI

The above is the output for the full adder. Here a ,b and c are the inputs and d,e are the sum and carry using GDI technique. Here the number of gates as well as power consumption is reduced when compared to CPL. GDI technique uses only a total of 10 transistors.

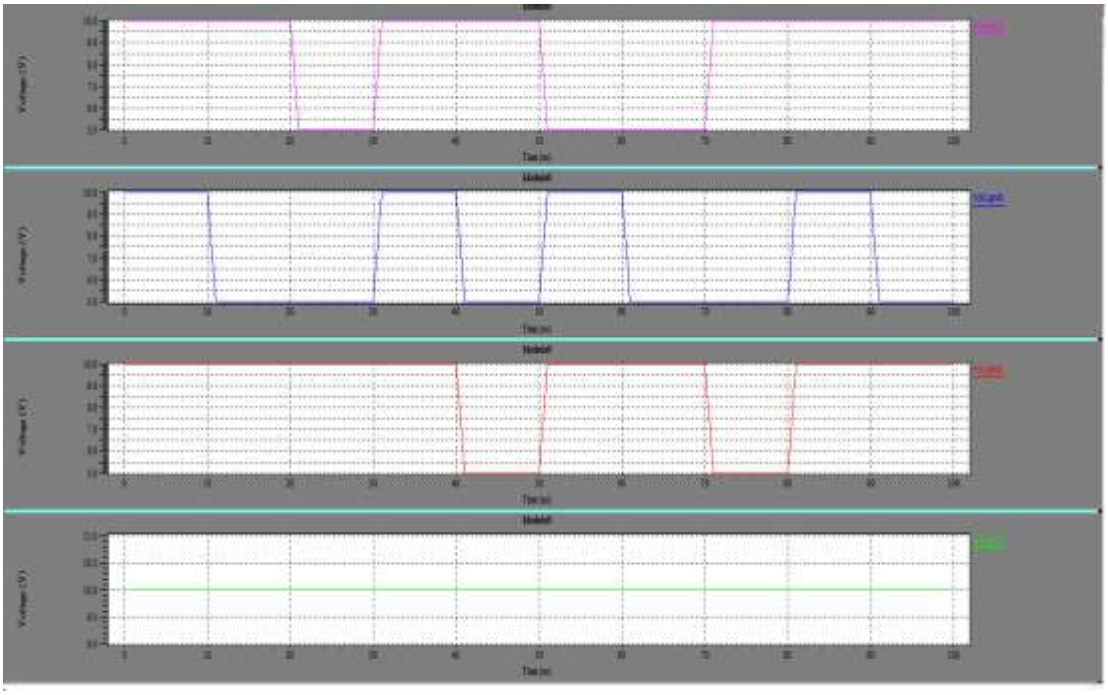

Figure 9. Waveform of Inputs a0 to a3 for Multiplier Using GDI

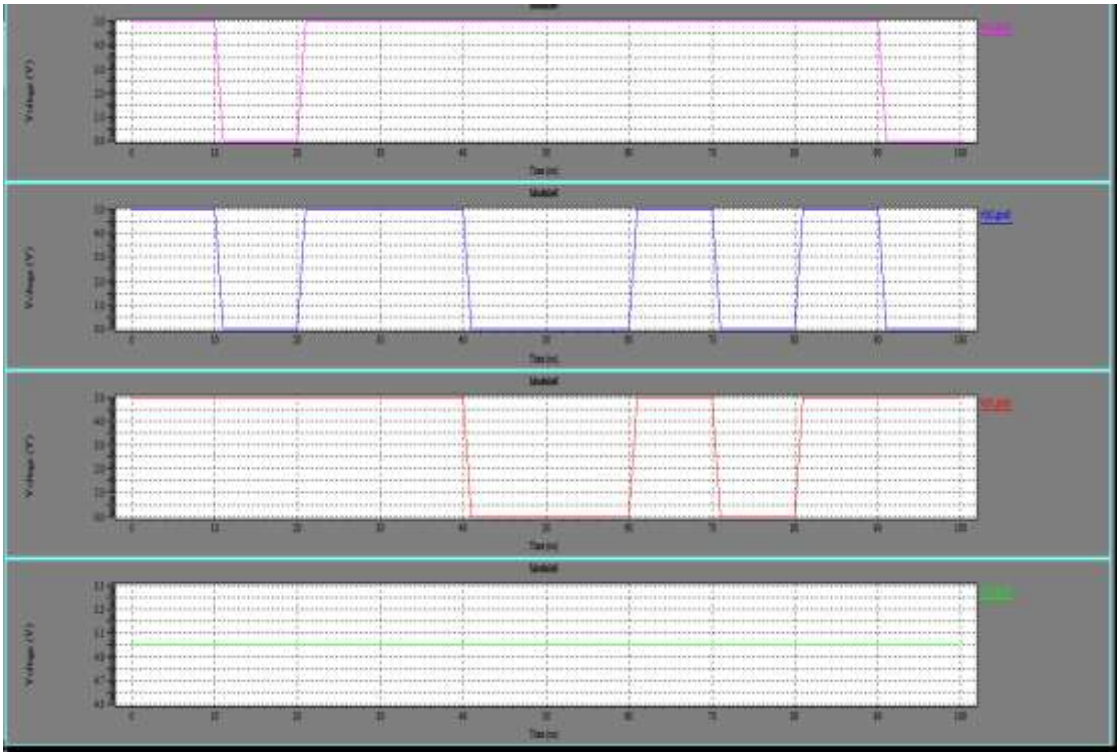

Figure 10. Waveform of Inputs b0 to b3 for Multiplier Using GDI

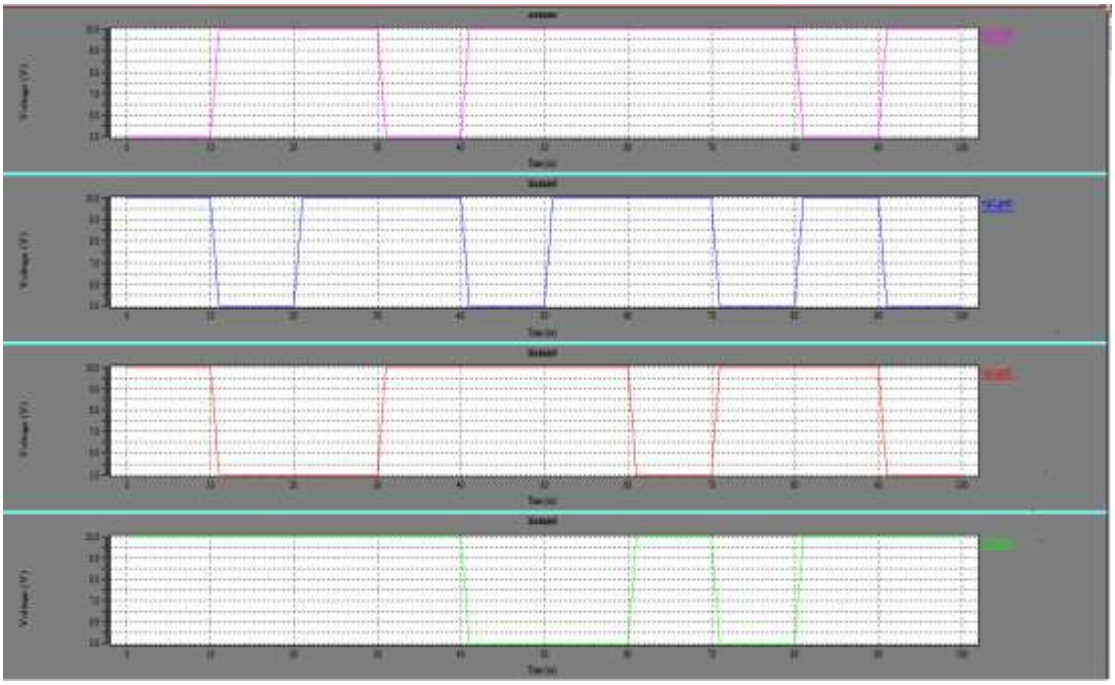

Figure 11. Waveform of Outputs p0 to p3 for Multiplier Using GDI

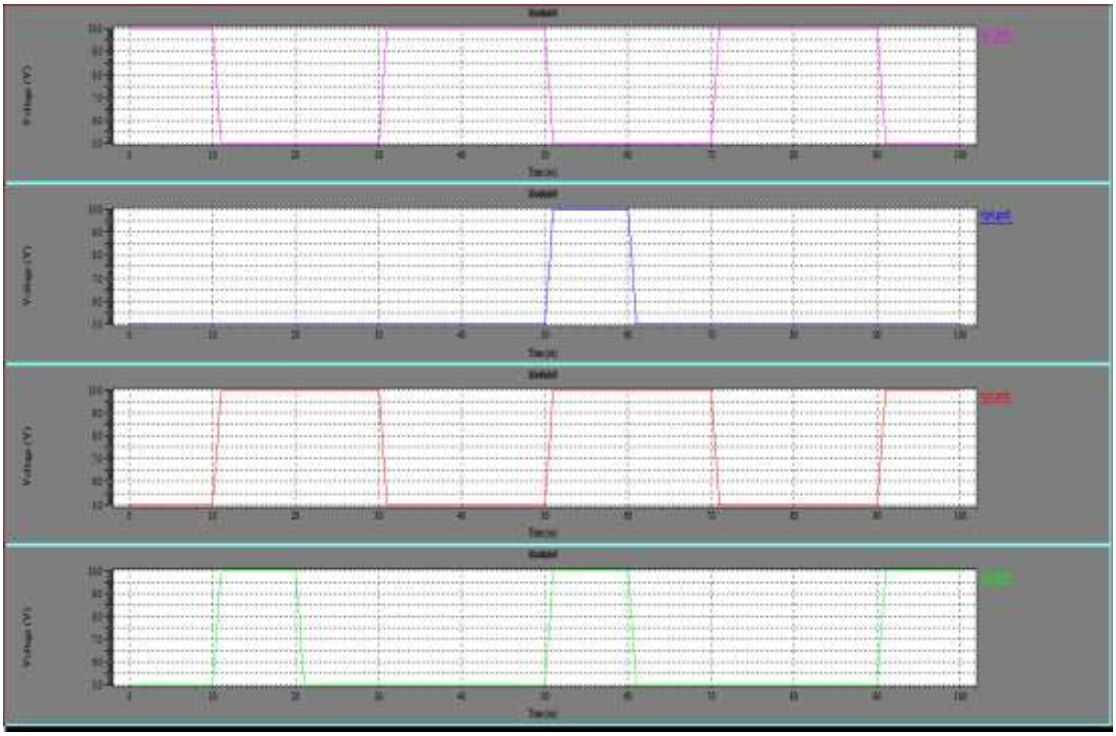

Figure 12. Waveform of Outputs p4 to p7 for Multiplier Using GDI

The figure 9 and 10 shows the input waveforms to the multiplier were the inputs are from a0 to a3 and b0 to b3.The output from p0 to p7 are show in figure 11 and 12 respectively**.**

V PERFORMANCE ANALYSIS

Comparison table depicts the transistor over a range of Power Supply and as it is shown in the proposed technique has minimum Power and transistor count

Table 5.1 COMPARISON OF FULL ADDER DESIGNS

PARAMETERS	CPL	GDI
TRANSISTOR COUNT(N)	18	10
MAXIMUM POWER(WATTS)	0.1179	0.002714

Table 5.2 COMPARISON TABLE FOR MULTIPLIERS

PARAMETERS	CPL	GDI
TRANSISTOR COUNT(N)	200	136
MAXIMUM POWER(WATTS)	1.4833	0.5373

VI CONCLUSION

The 4 bit Array multiplier is implemented by using GDI Technique and Complementary Pass Transistor Logic. Implementation as well as simulations are compared and carried out in tanner Software showing less power consumption in GDI circuit. From the comparison table, it is clear that GDI based multipliers has least power consumption at 5volt supply compared to Complementary Pass Transistor Logic (CPL). It is also most effective in

terms of number of transistors required.. Nowadays, chip area is very important parameter. With respect to chip area, GDI technique is significantly advantageous over other technique which cannot be calculated using tanner software. Calculation of area can be taken as future enhancement.

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