AN EFFICIENT VLSI IMPLEMENTATION FOR 64 BIT ERROR TOLERTANT ADDERS

A.Karthikeyan[1], V. Pradeep[2], G. Praveen Kumar[3], S. Lakshman[4]

[1]*Assistant professor, Department of Electronics and Communication Engineering, SNS college of Technology (India)*

[2,3,4] *Department of Electronics and Communication Engineering, SNS college of Technology (India)*

ABSTRACT

The adders are the basic elementary block which is used in most digital components.The probability of errors in the present VLSI technology is very high and it is increasing with technology scaling. In modern VLSI technology, the occurrence of all kinds of errors has become inevitable. The removal of all kinds errors is not an easy task and it is also not required for certain applications like image and video processing. For those certain applications approximate results are acceptable. Hence Error Tolerant Adder[ETA] is proposed for those certain applications which provide approximate result at a very high speed than other adders. ETA is an emerging concept in VLSI design. It uses logical OR operation for sertain LSB bits hence it produces greater efficiency. The proposed adder provides improvement in delay, area and as well as cost of accuracy. The ETA is able to ease the strict restriction on accuracy and at the same time improvements in power and speed performance. The construction of ETA is simple and it also easy to implement.

Index terms: Error Tolerant Adder (ETA)

I.INTRODUCTION

In general adder circuit the result produced will be accurate but it would not be more efficient and it will also consume more time, area and power. When we consider an error tolerant adder even though the results are approximate the area consumed and power consumption would be less when compared with other conventional adders. In most digital adder circuit the delay of the output is due the carry propagation involved in the internal process and so to avoid this carry propagation delay this circuit has been designed . This elimination of the carry propagation will definitely affect the output and hence these eliminations are avoided in the MSB and normal adder circuits have been implemented on some MSB. By this method error may take place in the any part of certain least significant bits and hence it not have a great impact on the accuracy of the result. In certain applications the accuracy of the adders need not be considered and so the error tolerant adder can be used in such cases. The system

which incorporates this design will generate acceptable results and it may contain defect In its internal process but the error produced will be only to a certain number of least significant bits which will never affect the accuracy of the results in a major level. In ETA only basic logic gates are used which eventually reduces the complexity of the design and it also used in reducing other factors including time and cost. The level of the tolerant is also high when compared with other adder circuits.

II.DESCRIPTION OF ERROR TOLERANT ADDER

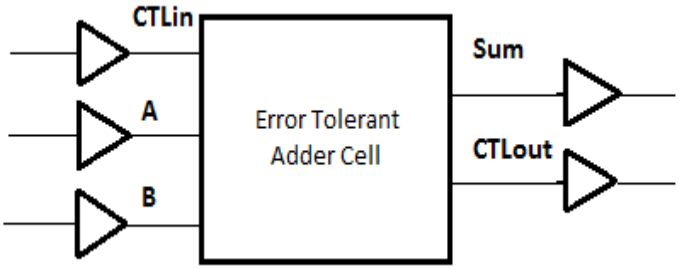

Fig 1: Error Tolerant Adder Cell

The above is the simple block diagram for the basic error tolerant adder cells. These adders perform only very basic addition using logic gates.

The usage of error tolerant has already been mentioned by comparing with the normal conventional adders. But there are few parameters through which we can calculate and obtain the approximate design for ETA. The following are the important parameters to calculate,

2.1 Calculation of Overall Error

The overall error is one of the important parameter to be considered. The overall error can be calculated using the formula,

OVERALL ERROR (OE): |Rc - Ra|, where Rc denotes the correct result and Ra denotes the approximate result. The difference between those two results will give us the overall error in the circuit.

ACCURACY: Accuracy is generally called as the true value which gives out the perfect output for the inputs given..

ACC = (1 − OE/Rc) × 100%, and ranges from 0% to 100%.

TOLERANT: The potential of the adder to avoid the errors is the tolerance level of the adder. ETA has very high tolerance level

III.OPERATION OF THE ERROR TOLERANT ADDER

The operation of the ETA is briefly explained using a figure given below. It consists of both accurate and as well as inaccurate part. The inaccurate part is the one which gives out the approximate result at a very minimum level.

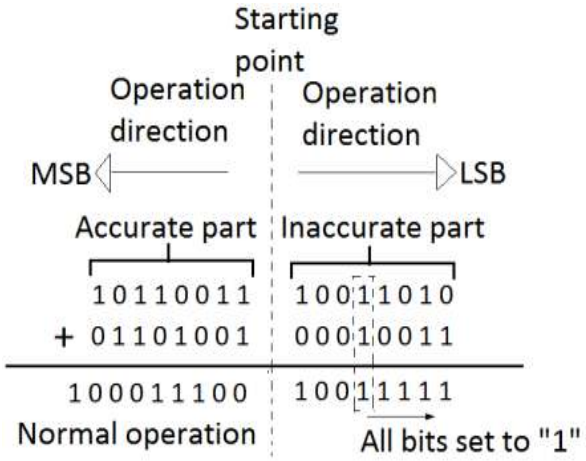

Fig 2: Operation Process Of ETA

The inaccurate part should be taken in the Least Significant Bit(LSB). The other MSB bits are bits are accurate which can be performed with some conventional adder. The LSB part which is considered as the inaccurate part is done with the simple AND and OR operation. The main function is that all the bits which are considered as inaccurate part should be set to 1 with the logical gate operation.

IV.IMPLEMENTING ETA IN HARDWARE

To implement ETA in hardware we need two different blocks namely addition block and control block. The addition block is used to perform a carry free addition and The control block is used to generate the control signals, to determine the working mode of the carry-free addition block.

4.1 Carry Free Addition Block

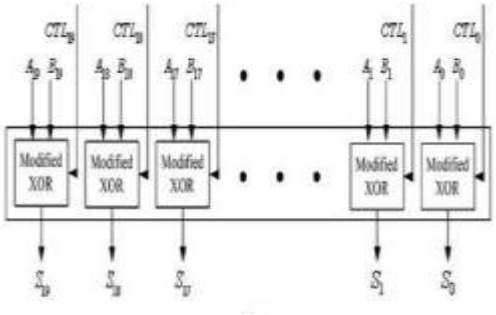

Fig 3: Carry Free Addition Block

The carry free addition is used to design the inaccurate part which is made of many different modified XOR gates which is showed in a block diagram above**.** In the modified XOR gate, three extra transistors, are added to a conventional XOR gate.

4.2 Control Block

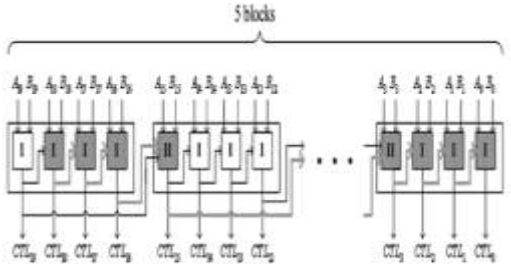

Fig 4: Control Block

The control block is to generate the clock signals for the carry free addition block**.**the control block is arranged into five equal-sized groups, with\additional connections between every two neighbouring groups. The control signal generated by the leftmost cell of each group is connected to the input of the leftmost cell in next group. The extra connections allow the propagated high control signal to "jump" from one group to another instead of passing through all the 20 cells. Hence, the worst case propagation path consists of only ten cells.

V.CONSTRUCTION AND PERFORMANCE OF OTHER ADDERS

When we consider other conventional adders their construct will also be found little complex. But the proposed design of ETA is simple to construct because it consists of only logical gates. The performance is also found to be good and efficient than other adders. But only small drawback is that it shows only approximate output for the particular number of least significant bits. Not only the performance increases it is area efficient, the time delay is less and the power consumption is less than other conventional adders

This proposed ETA is efficient and can be used in many places where approximate results are acceptable which will produce good result.

VI.DELAY ANALYSIS

In this design certain amount of Least Significant Bits of both inputs does not undergo normal addition. They are passed through some basic as mentioned earlier which when analysed has reduced the time delay and area consumption. This tremendous decrease in area and delay has made this adder an efficient and highly reliable. The delay analysis of 64 bit ETA has been clearly demonstrated with neat charts

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	62	66,560	1%
Number of occupied Slices	40	33,280	1%
Number of Slices containing only related logic	40	40	100%
Number of Slices containing unrelated logic	0	40	0%
Total Number of 4 input LUTs	62	66,560	1%
Number of bonded IOBs	96	633	15%
Average Fanout of Non-Clock Nets	1.88		

Maximum combinational path delay: 17.141ns

Fig 5: Utilization and time delay for 16 bit ETA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	31	66,560	1%
Number of occupied Slices	20	33,280	1%
Number of Slices containing only related logic	20	20	100%
Number of Slices containing unrelated logic	0	20	0%
Total Number of 4 input LUTs	31	66,560	1%
Number of bonded IOBs	49	633	7%
Average Fanout of Non-Clock Nets	1.87		

Maximum combinational path delay: 27.853ns

Fig 6: Utilization and time delay for 32 bit ETA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	124	66,560	1%
Number of occupied Slices	80	33,280	1%
Number of Slices containing only related logic	80	80	100%
Number of Slices containing unrelated logic	0	80	0%
Total Number of 4 input LUTs	124	66,560	1%
Number of bonded IOBs	192	633	30%
Average Fanout of Non-Clock Nets	1.88		

Maximum combinational path delay: 49.276ns

Fig 7: Utilization and time delay for 64 bit ETA

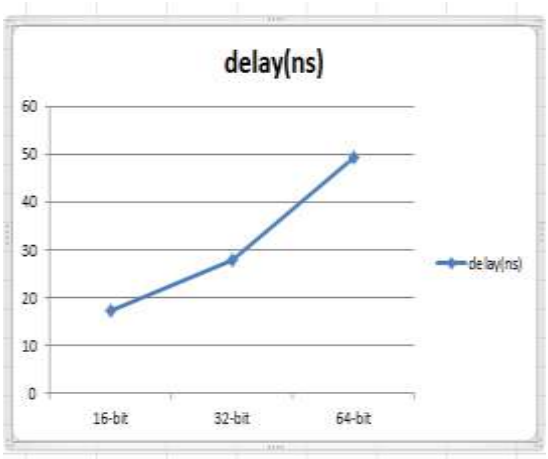

Fig 8: Overall delay analysis graph

VII.SIMULATION RESULTS

The simulation results for the above design clearly gives the approximate resu;lts from the addition of the given inputs which has been programmed using verilog HDL & Xilinx software overall power consumption of this 64 bit ETA IS 0000 watts and the memory is almost 167mb.

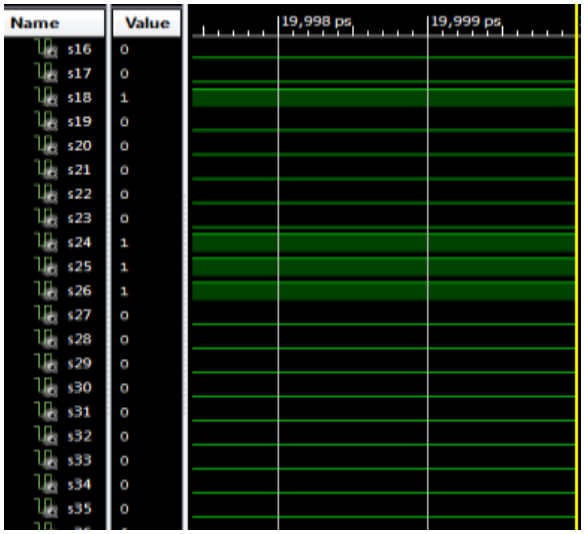

Fig 10: Simulation Results

VIII.CONCLUSION

In this paper , 64bit error tolerant adder has been designed using the verilog hdl and when compared with other adder it is clear that this design is more efficient and less power consuming. Even though it is superior in features than other adders it does not give accurate answers all the time and hence it is more suitable for the digital systems

where the speed is considered more than its accuracy. In digital systems this ETA can be implemented which will increase the performance of these systems. Our approach has been justified by the comparision made
With other conventional adders and result obtained by the Xilinx software

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AUTHORS PROFILE

KARTHIKEYAN.A. received his B.Tech., degree specialized in Electronics and Communication Engineering in Bharathiyar College of Technology, Karaikal in the year 2008 under Pondicherry University, Pondicherry, and M.E., degree in VLSI Design in SNS College of Technology, Coimbatore in the year 2012 under Anna University, Chennai. He is now working as Assistant Professor in the

Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamilnadu, India. His area of interest includes Wireless Sensor Networks, VLSI Design Techniques and Computer networking. He is a Life Member of the International Society for Research and Development (MISRD), International Association of Engineers (MIAENG) and International Association of Computer Science and Information Technology (MIACSIT).

V.**Pradeep** pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design, PIC microcontroller and Automation

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G.Praveen kumar pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design, PIC microcontroller and Arduino programming.

LAKSHMANAN.S pursuing B.E Electronics and Communication Engineering at SNS College of Technology ,Coimbatore .His areas of interest are VLSI system design , wireless communication systems and robotics designing.