DESIGN OF COMPRESSOR USING CMOS 1-BIT FULL ADDER

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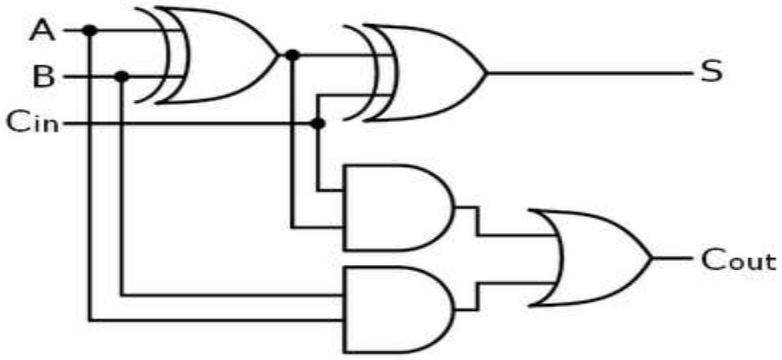
ABSTRACT

An adder determines the overall performance of the circuits in Very Large-Scale Integration (VLSI) systems . 1-bit full adder is a very great part in the design of application particular Integrated circuits. Power consumption is one of the most significant parameters of full adders. Therefore reducing power consumption in full adders is very important in low power circuits. This paper presents a new low power full adder based on a new logic approach, which reduces power consumption by implementing full adder using 3T XOR module and 2-to-1 multiplexer, with 8 transistor in total, named CBFA(CMOS Based Full Adder)-8T. The role of full adders plays an important role in designing a multiplier. A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. The 4-2 compressor has been widely employed in the high speed multipliers for the construction of Wallace tree to lower the delay of the partial product accumulation stage. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. The results show that the proposed circuit has the lowest power-delay product with a significant improvement in silicon area and delay.

I INTRODUCTION

1.1 ADDER



Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Adders serves as a main building block for synthesis and all other arithmetic

operations. The efficient implementation of an arithmetic unit and the binary adder structures become a very critical hardware unit. A full adder shown in Figure 1 is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, both of which are binary digits

1.2 Power Considerations

The aim to design the system for low power is not a straight forward task, as it is involved in all the IC-design stages.There are several sources of power consumption in CMOS circuits.

- Switching Power: Due to output switching during output transitions.
- Short Circuit Power: Due to the current between VDD and GND during a transistor switching.
- Static Power: Caused by leakage current and static current.

1.3 Requirements for Design of FA

- Output and input capacitances should be low to reduce dynamic power. Therefore, fewer nodes should be connected to SUM and COUT signals.
- Avoid using inverters will reduce switching activity and static power.
- Avoid using both VDD and GND simultaneously in circuit components. It can reduce short circuit and static power.
- Using Pass transistors usually lead to low transistor count full adders with low power consumption. However, sometimes pass transistor full adders have not full swing outputs due to threshold loss problem.
- PMOS cannot pass logic 0 and NMOS cannot pass logic1 completely. Uncompleted swing reduces dynamic power but sometimes increases leakage power, because transistors do not turn off completely by poor signals.
- Most important components of the power consumption in full adders are the XOR and XNOR gates. Therefore, more work should be done to reduce transistor count and power of these components or completely omit them.
- Reducing number of transistors usually lead to reduce the power in full adders. However, sometimes it does not improve PDP. Therefore, reducing transistor counts does not always lead to reduce in PDP or power consumption.

II EXISTING METHODS

2.1 Design of Full Adder

Addition is the most commonly used arithmetic operation in microprocessors and DSPs, and it is often one of the speed-limiting elements. Hence optimization of the adder both in terms of speed and power consumption should be pursued.During the design of an adder there are two choices in regard to different design abstraction levels.

One is responsible for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the specific design style at transistor level to implement the one-bit full adder. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area .

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the next less significant stage.

The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The circuit produces a two-bit output sum typically represented by the signals C_{out} and S.

A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and or the two carry outputs is shown in the figure 2.1.

Equivalently, S could be made the three-bit xor of A, B, and Cin and Co could be made the three-bit majority function of A, B, and Cin. The output of the full adder is the two-bit arithmetic sum of three one-bit numbers.

SUM=A XOR B XOR Cin ----------Equ(2.1)

Cout=(A AND B)OR(B AND Cin)OR(Cin AND A) ----------Equ(2.2)

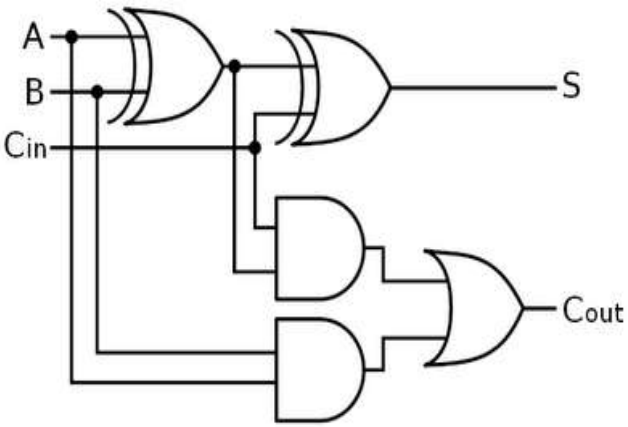


Figure 2.1 Logic diagram of Full Adder

A full adder is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and carry value, which are both binary digits.The truth table for full adder circuit is shown in the table 2.1

TABLE 3.1 Truth table of Full Adder

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The role of full adders in arithmetic circuits can be classified into two categories .

- The chain structured such as ripple carry adders and array multipliers. In these applications, the critical path often traverses from the carry input to the carry output of the full adders. It is demanded that the generation of the carry-out signal is fast. Otherwise, the slower carry-out generation will not only extend the worst case delay, but also create more glitches in the later stages, hence, consume more power.
- The tree structured, which is frequently used in multipliers.

2.2 Full Adder Using 16T

It is the same as New-13T in terms of the output modules as shown in the figure 2.2. However, the XOR-XNOR module has been modified to reduce delay and power consumption. The XOR-XNOR modules does not have full-swing outputs thus, the transistors which have been connected to this module are turned on or off slowly.

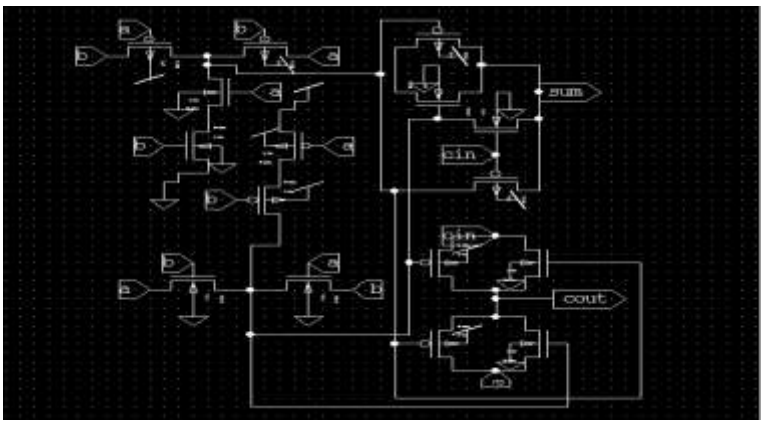


Figure 2.2 Schematic 16T Full Adder

2.3 FULL ADDER USING 12T

12T has been implemented using six multiplexers and 12 transistors.From figure 2.3 it is seen that each multiplexer is implemented by pass-transistor logic with two transistors. There is no VDD or GND connection in this circuit and there are some paths containing three serried transistors.

It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

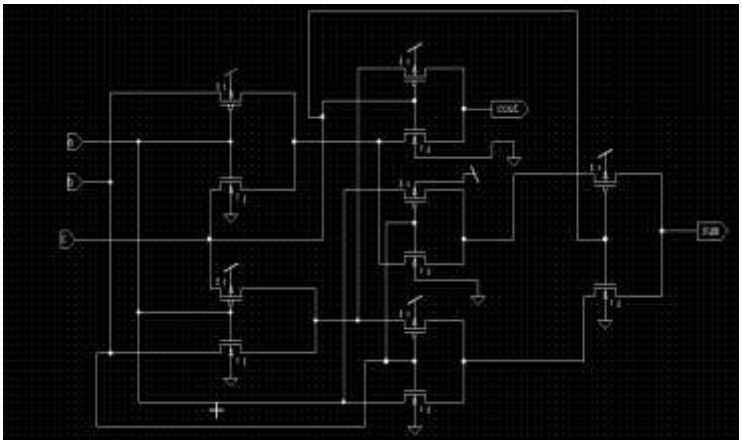


Figure 2.3 Schematic 12T Full Adder

2.4 FULL ADDER USING 10T

A full adder in form of centralized structure is made by ten-transistor-10T as shown in the figure 2.4.In this sum and cout are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic.

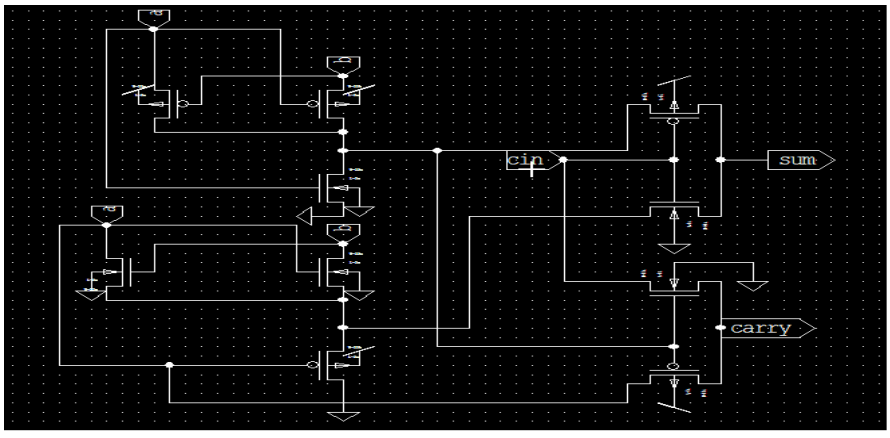


Figure 2.4 Schematic 10T Full Adder

III PROPOSED METHOD

3.1 Full Adder Using 3T XOR AND 2:1 MUX

Full adder circuit can be implemented with different combinations of XOR, XNOR and 2x1 multiplexer blocks. The goal of this paper is to design a high performance and low power full adder module with 8T.

Compared to the various logic structures, the proposed Full Adders embodies only 8 transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the power consumption is reduced to a great extent. The proposed 8T full adder is based on XOR logic constructed using two 3T XOR cells and one multiplexer.Two XOR gates generate the sum and 2T multiplexer block generate Cout.

3.2 Design of 3T XOR Gate

The design of the full adder is based on the design of the XOR gate. The proposed design of full adder uses three transistor XOR gate .The design of a three transistor XOR gate is shown in figure 3.1.The design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter.

Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled and the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a 2 input XOR gate. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output Y is degraded with respect to the input.

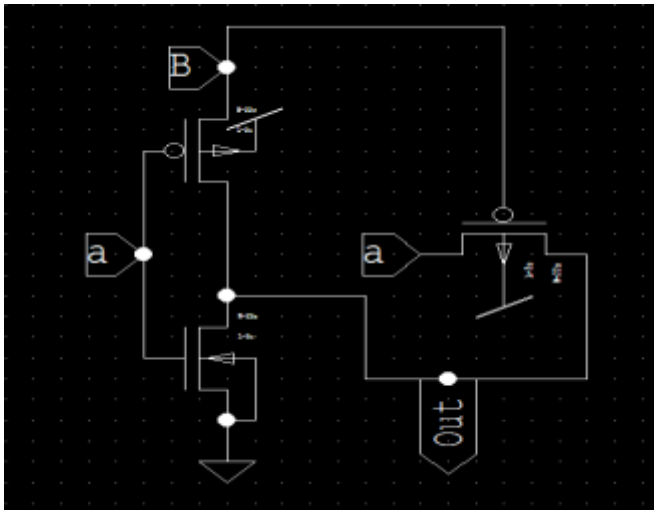


Figure 3.2 Schematic of 3T XOR

3.3 Design of 2:1 MUX

For our proposed full adder circuit, the possible circuit design for the 2-to-1 multiplexer is given the figure 3.3.In this, pass transistors are used in lieu of the transmission gate to reduce the circuit complexity**.**

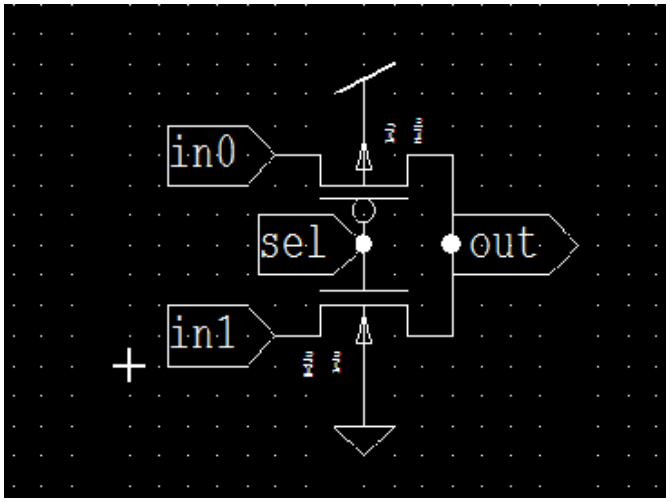


Figure 3.3 Schematic of 2:1 MUX

3.4 Block Diagram of Proposing FA

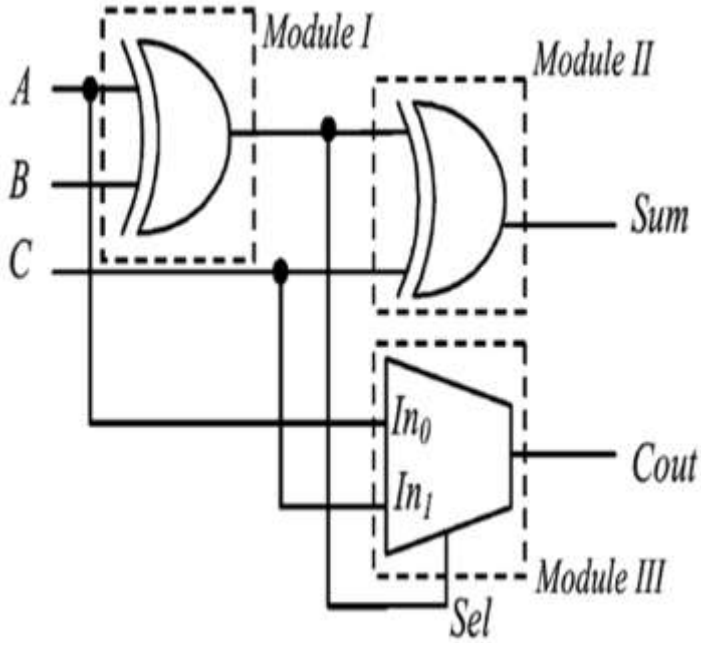


Figure 3.4 Proposed FA

The block diagram of the proposed full adder consists of three modules as shown in the figure 3.4.

Module 1:The xor operation of the input A and B is done.

Module 2: The xor operation of the output of A XOR B and the input C takes place.

Module 3:Finally the 2:1 mux operation happens based on the selection line.

3.5 Circuit Diagram

The circuit diagram of the eight transistor full adder is shown in figure 4.4 . The sum output is basically obtained by a cascaded exclusive ORing of the three inputs The carry output is obtained and the final sum of the products is obtained using a wired OR logic.

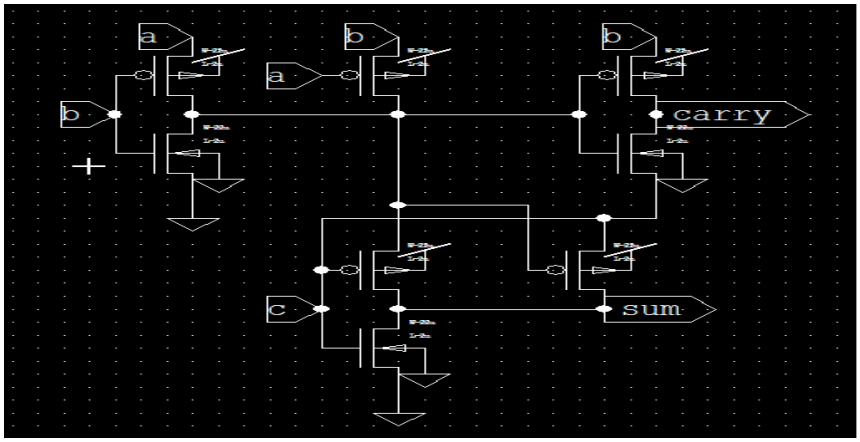


Figure 3.5 Full Adder using 8T

3.6 Design of Compressor Using 8T FA

A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier.

The 4-2 compressor has been widely employed in the high speed multipliers for the construction of Wallace tree to lower the delay of the partial product accumulation stage . The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing.

3.7 Block Diagram of 4-2 Compressor

A 4:2 compressor consists of five inputs and three outputs. It is called compressor, since it compress four partialproducts into two. This can be implemented with two stages of full adders (FA) connected in series.

This shows the logic decomposition of 4-2 compressor architecture. It is mainly consisted of six modules, four of which are XOR circuits and the other two are 2:1 MUX.The input variables in Fig. 3 are denoted by x1, x2, x3, x4, and cin.

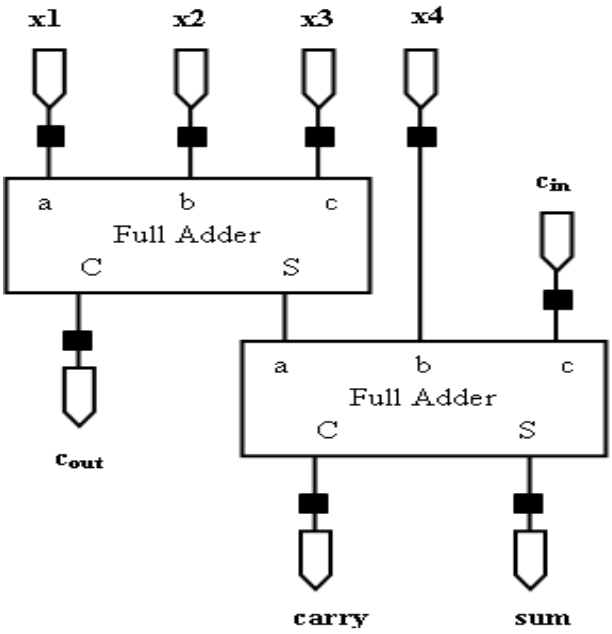


Figure 3.7 Block diagram of 4:2 Compressor

3.8 Logic Diagram and Operation of 4-2 Compressor

The design of 4-2 compressor is based on modified set of equations for the cout, sum and carry outputs as;

$$sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus cin \quad (3)$$

$$cout = x1 \oplus x2\ x3 + x1x2 \quad (4)$$

$$carry = (x1 \oplus x2 \oplus x3 \oplus x4)\ cin + (x1 \oplus x2 \oplus x3)\ x4 \quad (4)$$

The carry output (cout) is connected to the carry input (cin) of the next 4-2 compressor. Without propagating the carry to the higher bit, the 4-2 compressor can add four partial products because the carry output (cout) does not depend on the carry input (cin). This makes it a carry-free adder stage.

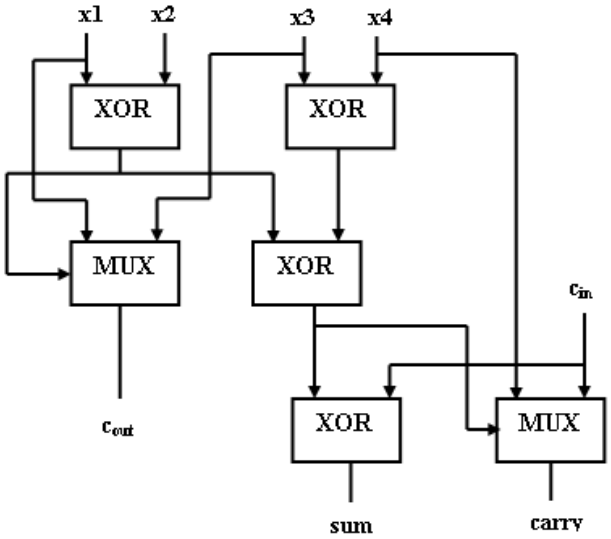


Figure 3.9 Logic diagram of 4:2 Compressor

Figure 3.9 shows the logic decomposition of 4-2 compressor architecture. It is mainly consisted of six modules, four of which are XOR circuits and the other two are 2:1 MUX.

3.10 Proposed Circuit

The proposed circuit of compressor consists of full adder of 8T which is based on modified CMOS inverter and PMOS pass transistor.

The inputs are named as x1,x2,x3,x4,cin and the outputs are given as cout,sum,carry.

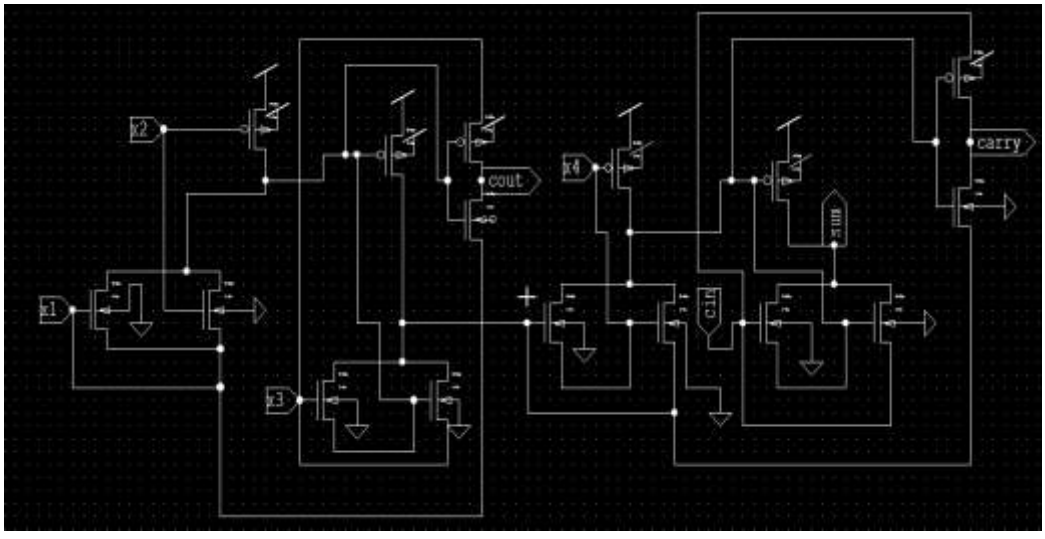


Figure 3.10 Schematic of 4:2 Compressor

From the figure 3.10 it is seen that XOR gates are used with multiplexers and they represent the combination of two full adder structure.

IV SIMULATION RESULTS

4.1 FA Using 16T

Using Tanner EDA software the simulations of different types of full adders are carried out and output waveform for the full adder is shown in the figure 6.1

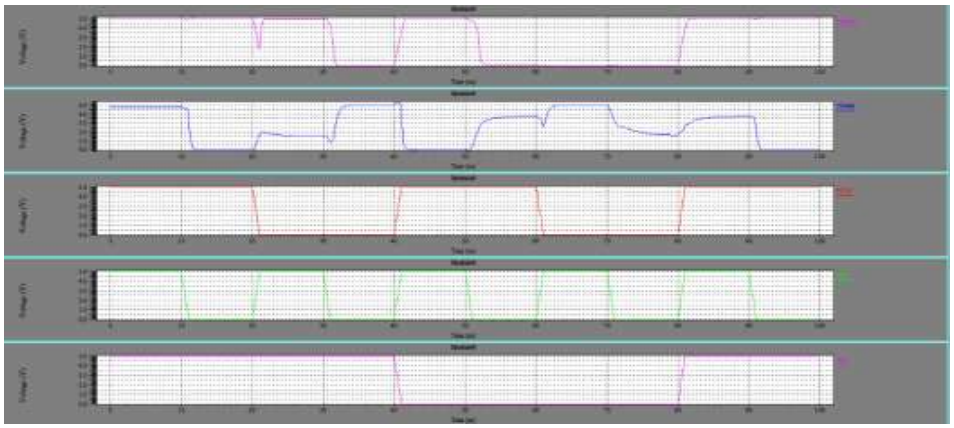


Figure 6.1 Output waveform of 16T FA

The power consumed by the circuit is shown in the figure 6

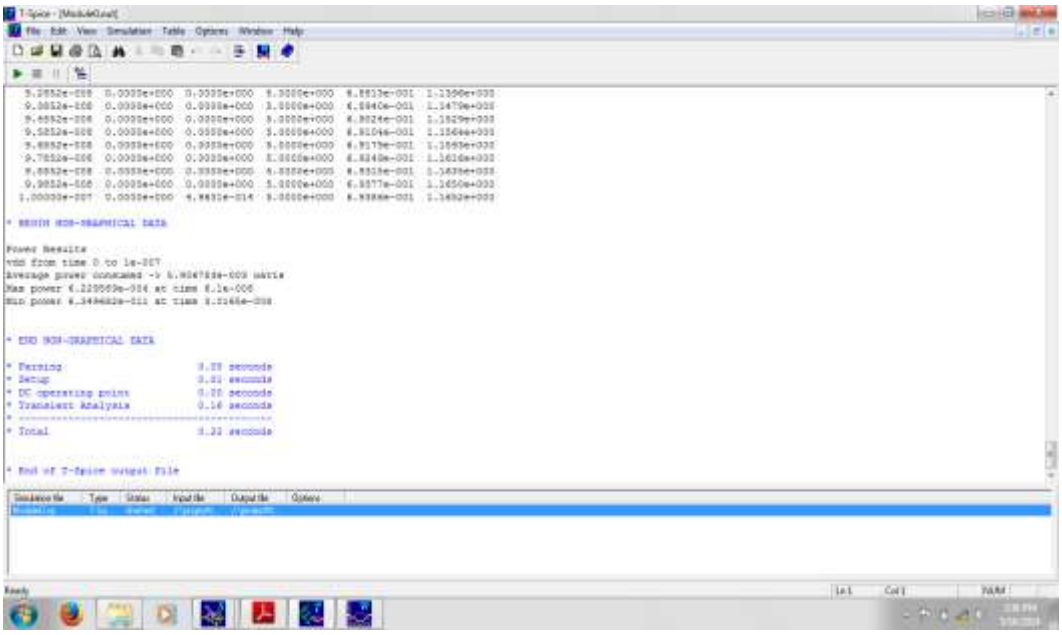


Figure 6.2 Power Output of 16T

6.2 FA Using 12T

12T full adder does the XOR operation for the input a, b and c and do the corresponding operation of carry.

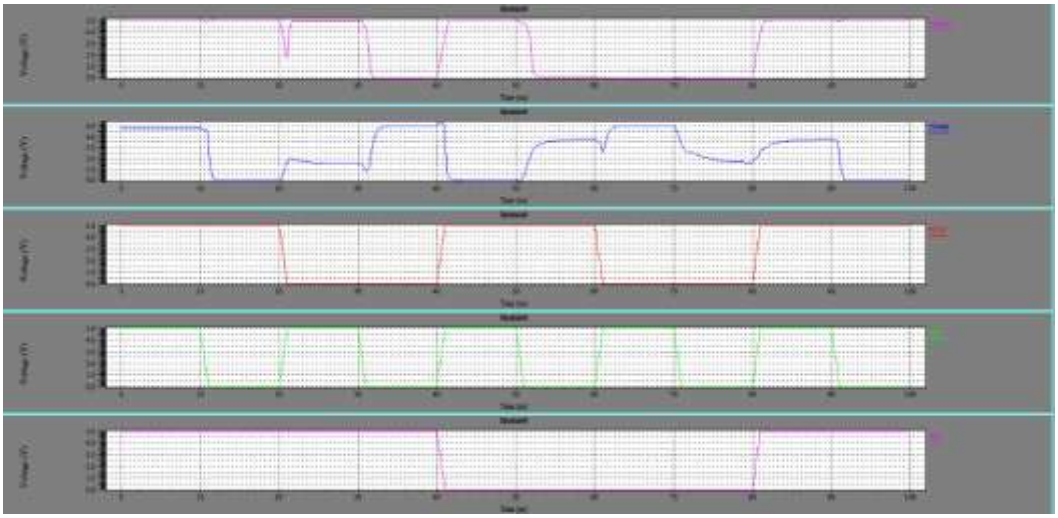


Figure 6.3 Output waveform of 12T FA

The power output of 12T is lesser than compared with the 16T andit is clear from the figure 6.4.

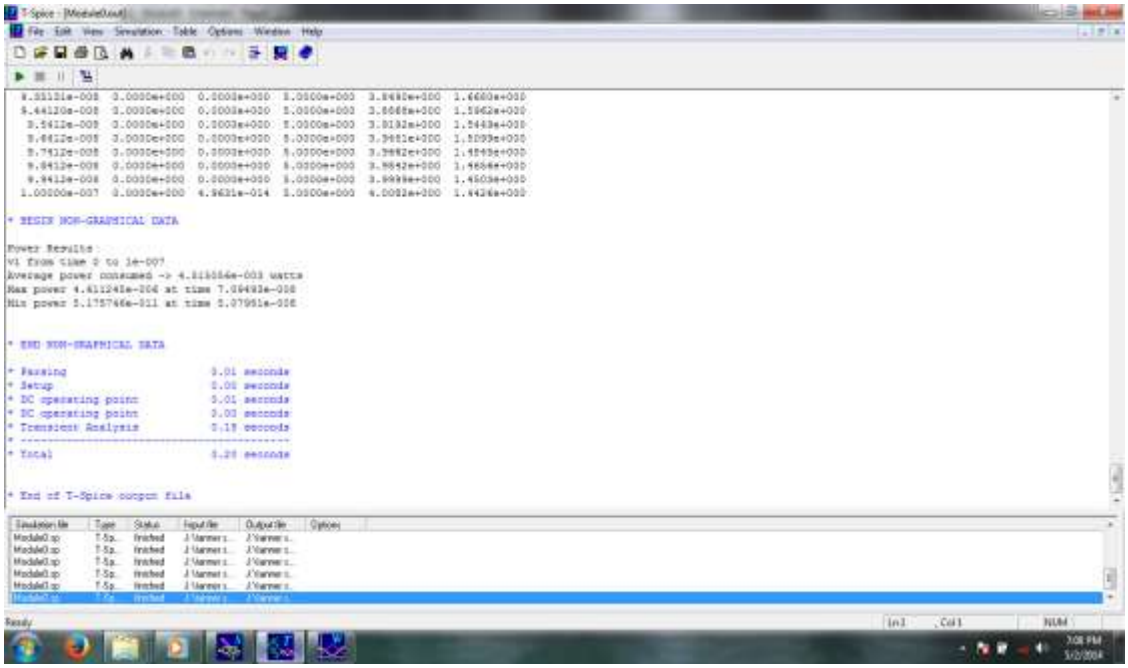


Figure 6.4 Power Output of 12T

6.3 FA Using 10T

10T full adders gives better performance than above full adders.

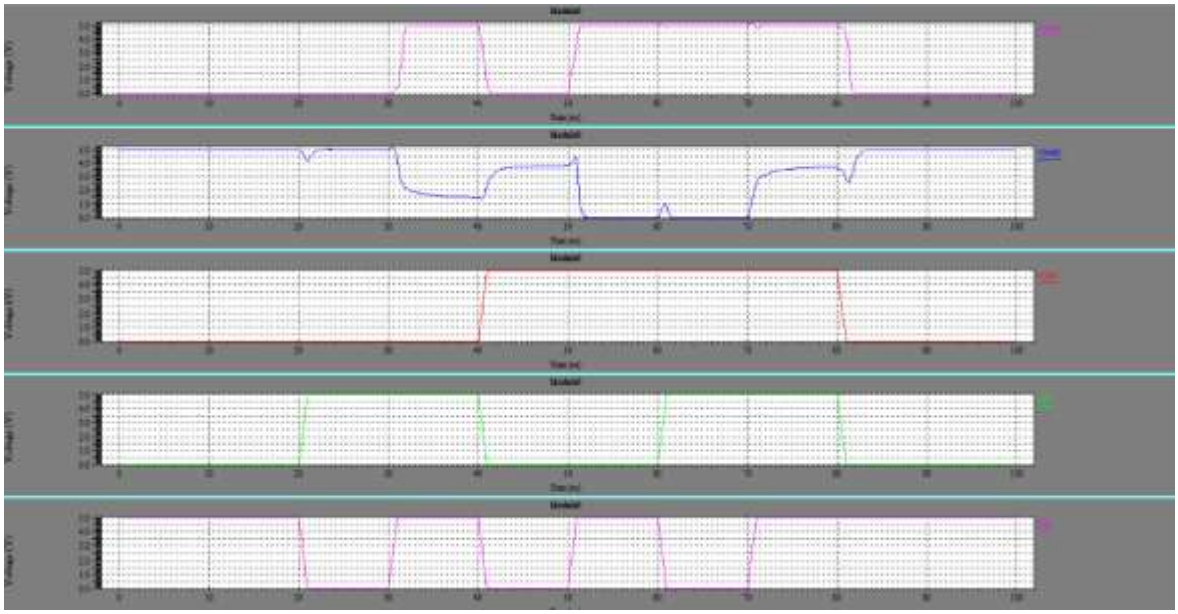


Figure 6.5 Output waveform of 10T FA

The power output is reduced greatly in 10T compared with that of other adders.

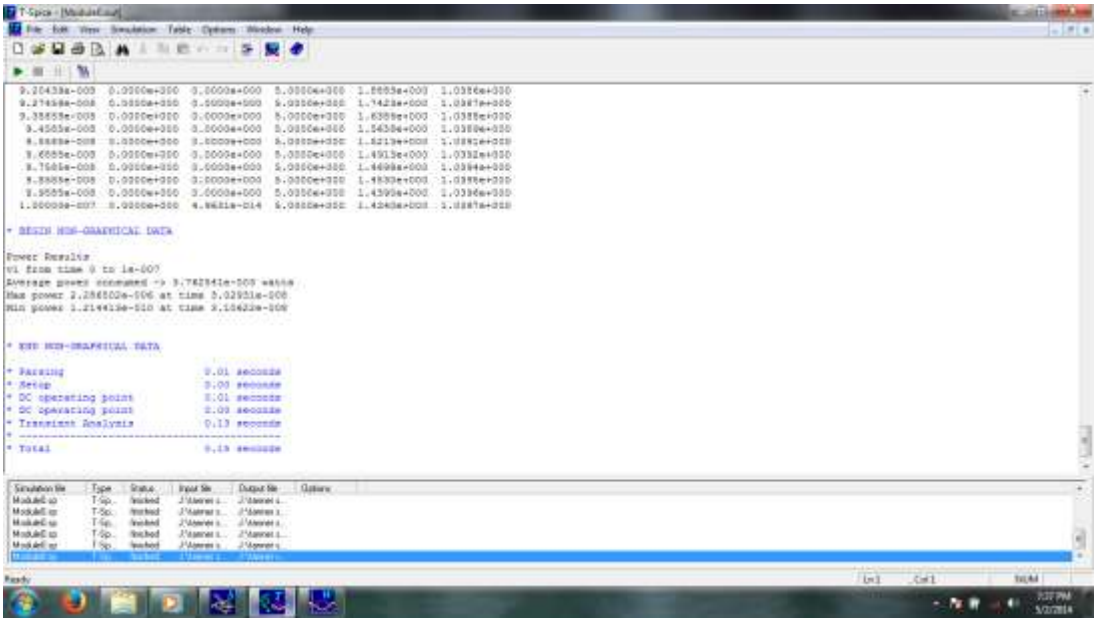


Figure 6.6 Power Output of 10T

6.4 FA Using 8T

The proposed full adder shows reduction in number of transistors compared to all the above existing structures.

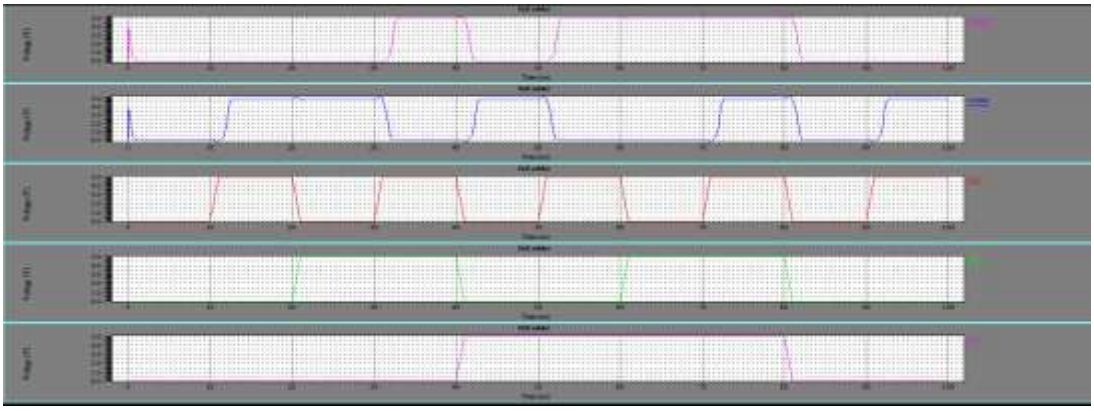


Figure 6.7 Output waveform of 8T FA

The power and the delay of the proposed circuit is greatly reduced and so this is used in the design of compressor**.**

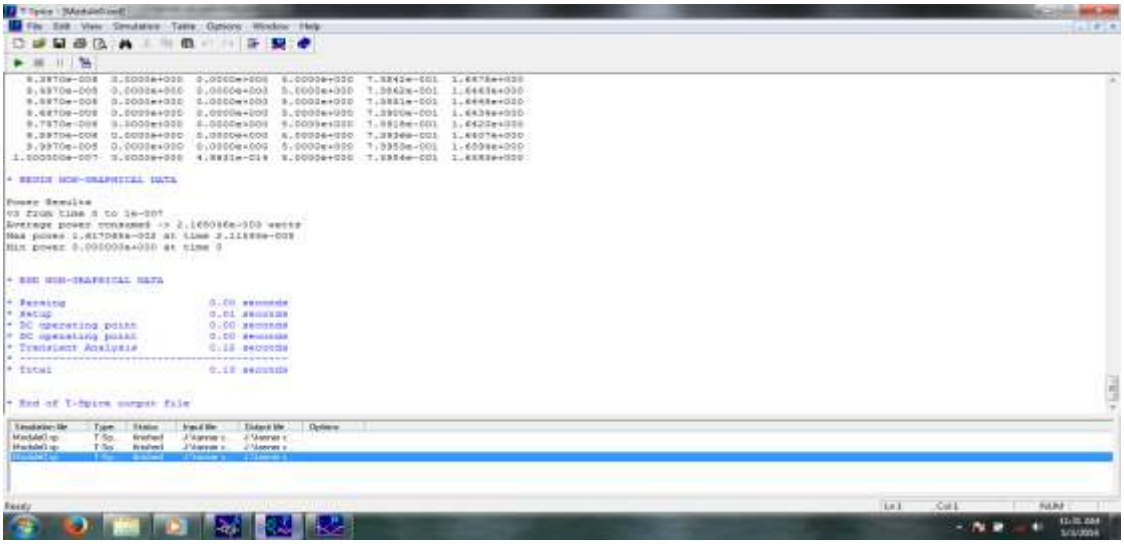


Figure 6.8 Power Output of 8T

6.5 Comparison Table of Various Full Adders

Table 6.1 Comparison Table

PARAMETERS	16T	12T	10T	8T
POWER(W)	0.29	0.22	0.21	0.18
DELAY(ns)	1.64	1.46	4.92	1.09
PDP(pJ)	475.6	321.2	1033.2	196.2

By comparing the various full adders 8T has significant power delay product and the number of transistors is also reduced highly.Hence it is used in the design of compressor.

6.6 Output Waveform of 4:2 Compressors

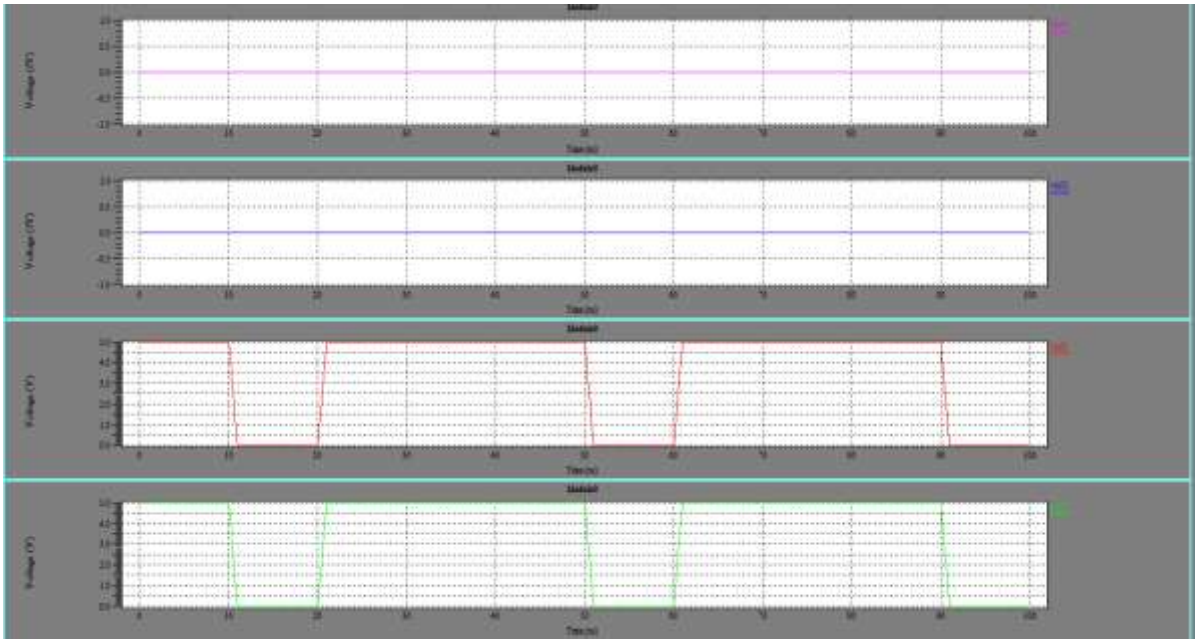


Figure 6.9 Input Waveform of Compressor

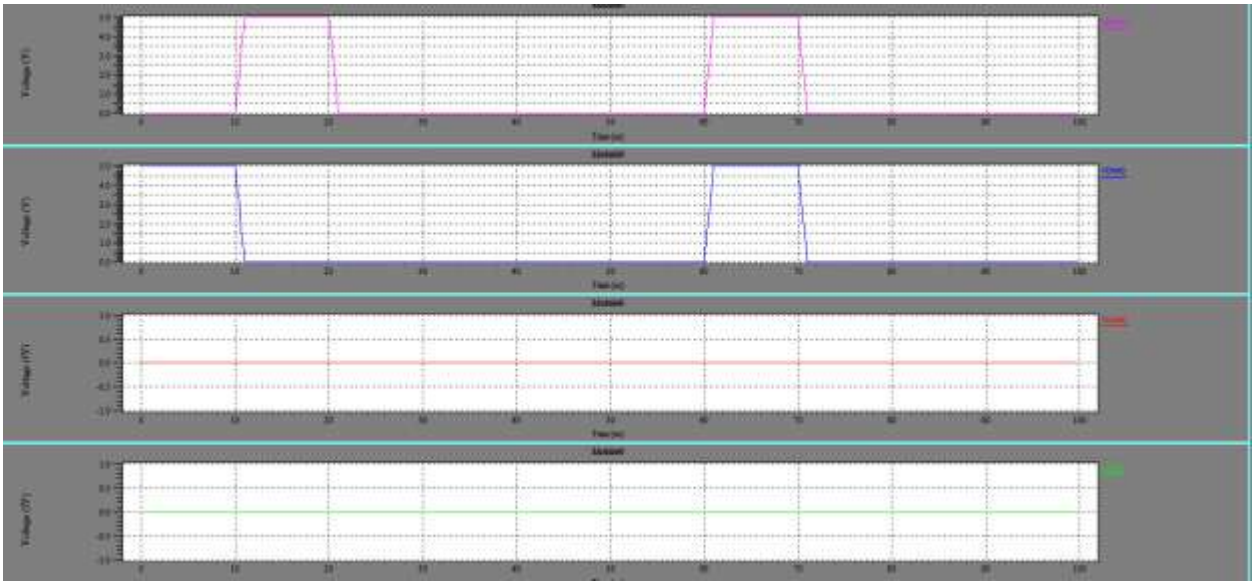


Figure 6.10 Output Waveform of Compressor

For the compressor circuit the inputs are given as x1,x2,x3,x4,cin and the corresponding output waveform cout,sum,carry are generated.