DESIGN OF ADVANCED HIGH-PERFORMANCE BUS TO INCREASE THE BIT RATE OF SECURED DIGITAL HOST CONTROLLER

S.Mathan Prasad[1], E.Abinaya[1], Dr. D. Somasundareswari[2]

[1,2] PG Student/ VLSI Design, SNS College of Technology, Coimbatore, (India)

[2]Dean and HOD, Department of ECE, SNS College of Technology, Coimbatore, (India)

ABSTRACT

Portable storage devices are becoming popular and growing rapidly. These devices can store and acquire information wherever and whenever you need. The important applications of portable storage devices are to make backup copies of important data, to share information between different computers or persons, and to secure information which are extremely confidential. But the drawback of handling these portable devices is, it has less read and write speed while transferring the data. This drawback can be overcome by increasing the bit rate between SD Host system and SD Memory card sockets. By changing the FSM control of AHB master, the speed of read and write operation is increased. Due to this the FIFO is controlled. In this paper the control signals between Advanced High-performance Bus Master and slave using Burst Transfer method and its performance is analyzed. The Burst Transfer method has some of the processing delay in its FSM. By using Split Transaction method the delay process that occurs in Burst Transfer method is rectified and increased the speed of the bit rate between SD Host system and SD Memory socket.

Keywords : Advanced High-performance Bus, Bit-rate, Finite State Machine, Host controller, Secured digital.

I INTRODUCTION

With the increasing consumer digital content, demand for high capacity digital storage is increasing rapidly. Today, portable storage media are widely used in all mobile phones, digital cameras, camcorders, and in many multimedia devices. Different memory formats like Flash, Secure Digital (SD), Compact Flash, Universal Serial Bus (USB), and Multimedia Card (MMC) are available in the market to store the digital contents. Of all these formats, SD provides many advantages over other formats. Secure Digital (SD) is a Non-volatile memory card format developed by the SD CARD Association (SDA) for use in portable devices. SD cards provide high storage capacity, higher transfer speed, and interoperability with Personal Computer (PC) - related devices and multimedia products.

The Host Controller handles SDIO/SD Protocol at transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bit, and checking for transaction format correctness. The Host Controller provides

Programmed IO method and DMA data transfer method. In programmed IO method, the ARM processor transfers data using the Buffer Data Port Register.

II. ARCHITECTURE OF SD HOST CONTROLLER

The SD3.0 / SDIO3.0 / eMMC4.5 Host Controller (3MCR Host Controller) is a Host Controller with an ARM processor interface. This product conforms to SD Host Controller Standard Specification Version 3.00. The block diagram of Host Controller is shown below in fig 1.

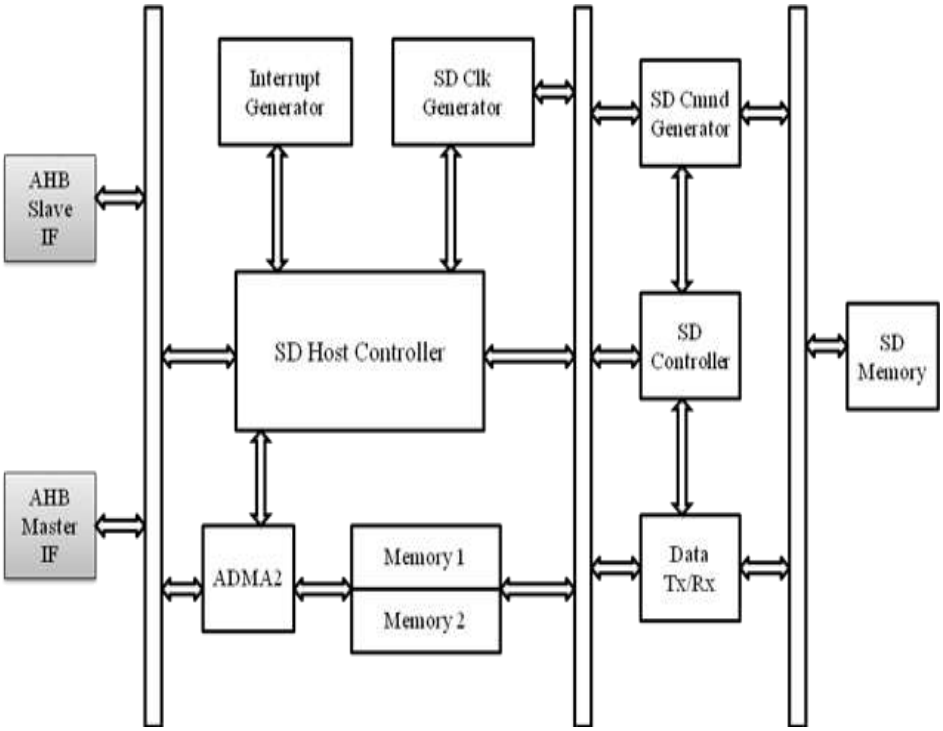

Fig.1 Block Diagram of SD Host Controller

2.1 Data FIFO

The SD/SDIO Host Controller uses one 1k dual port FIFO for performing both read and write transactions. During a write transaction (data transferred from ARM Processor to SD3.0 / SDIO3.0 / eMMC4.41 card), the data will be filled in to the first and second half of the FIFO alternatively. When data from first half of FIFO is transferring to the SD3.0 / SDIO3.0 / eMMC4.41 card, the second half of FIFO will be filled and vice versa. The two halves of the FIFO's are alternatively used to store data which will give maximum throughput. During a read transaction (data transferred from SD3.0 / SDIO3.0 / eMMC4.41 card to ARM Processor), the data from SD3.0 / SDIO3.0 / eMMC4.41 card will be written in to the two halves of the FIFO alternatively. When data from one half of the FIFO is transferring to the ARM Processor, the second half of the FIFO will be filled and vice versa and thereby the throughput will be maximum. If the Host controller cannot accept any data from SD3.0 / SDIO3.0 / eMMC4.41 card, then it will issue read wait to stop the data transfer from card or by stopping the clock.

2.2 Data Control Logic

The DAT [0-7] control logic block transmits data on the data lines during write transaction and receives data from the data lines during read transaction. The DAT [0-7] control logic block transmits data in the data lines on posedge and negedge of the SD CLOCK during DDR mode of operation. The DATA [0-7] receiver block receives/ samples the data on the data lines in both posedge and negedge of the SD CLOCK during DDR mode of operation. The Command control logic block sends the command on the cmd line and receives the response coming from the SD3.0 / SDIO3.0 / eMMC4.41 card.

III. ADVANCED HIGH PERFORMANCE BUS

The APB is part of the AMBA hierarchy of buses and is optimized for minimal power consumption and reduced interface complexity. The AMBA APB appears as a local secondary bus that is encapsulated as a single AHB or ASB slave device. APB provides a low-power extension to the system bus which builds on AHB or ASB signals directly.

Fig 2 shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master.

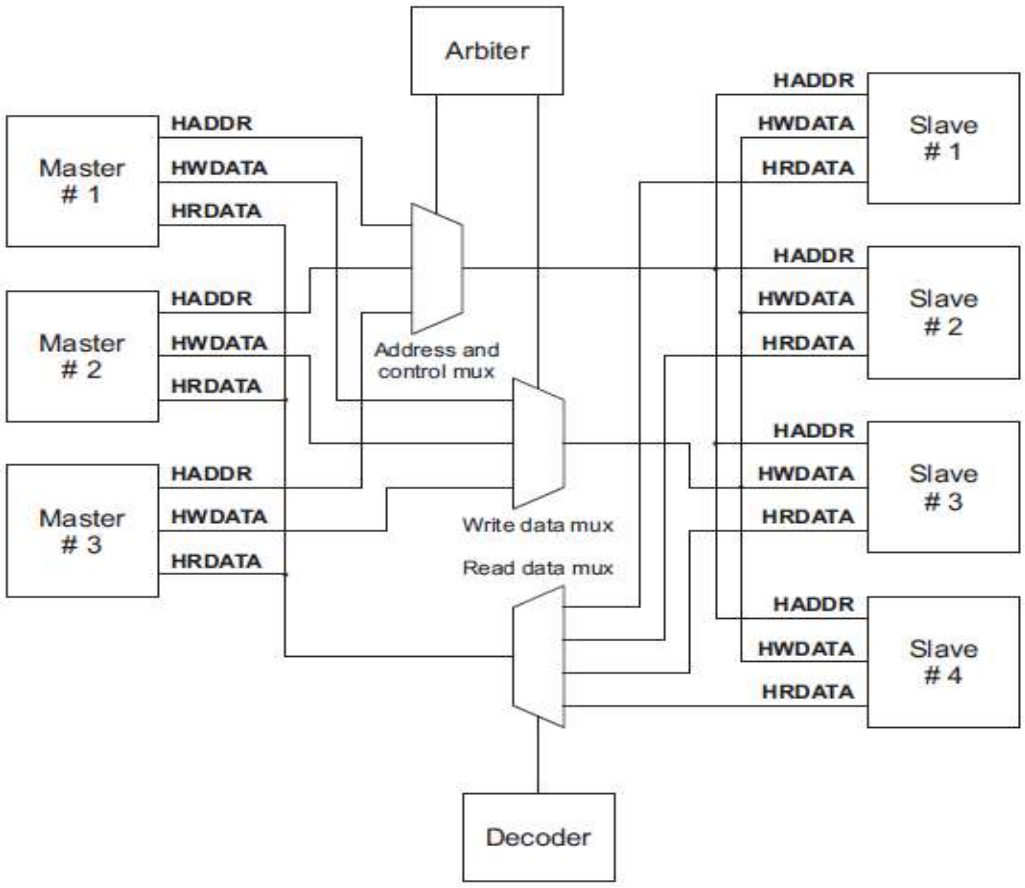

Fig.2 AHB-Lite Block Diagram

3.1 Advanced High-performance Bus Master

A bus master is able to initiate read and write operations by providing an address and control information. Only one bus master is allowed to actively use the bus at any one time.

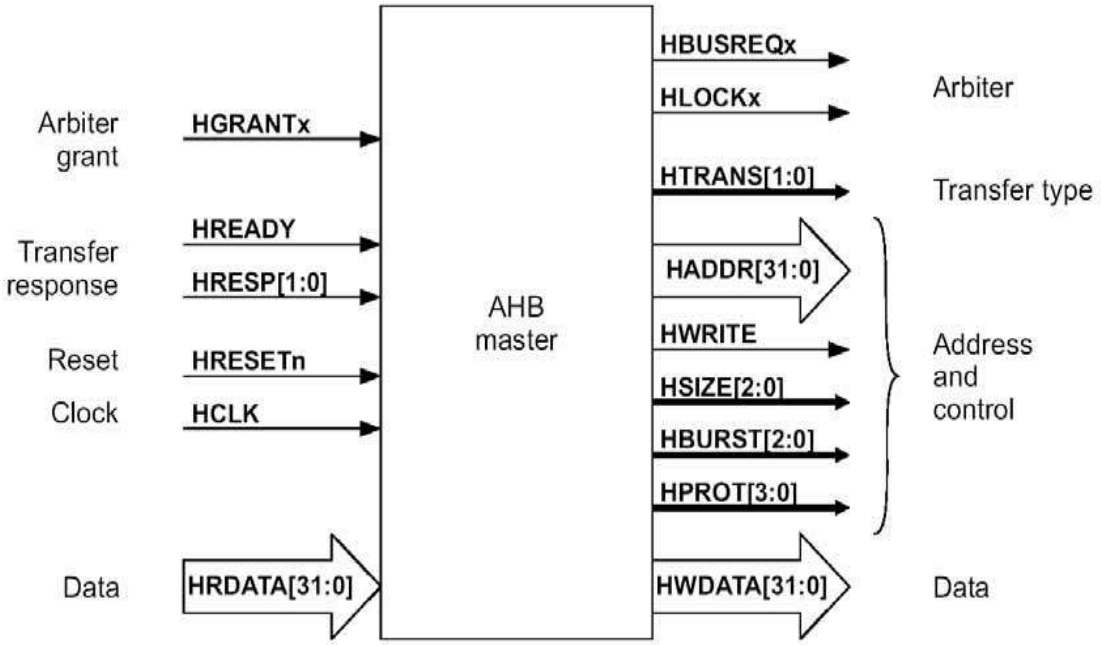

Fig. 3 AHB-Master Interface Diagram

3.2 Advanced High-performance Bus Slave

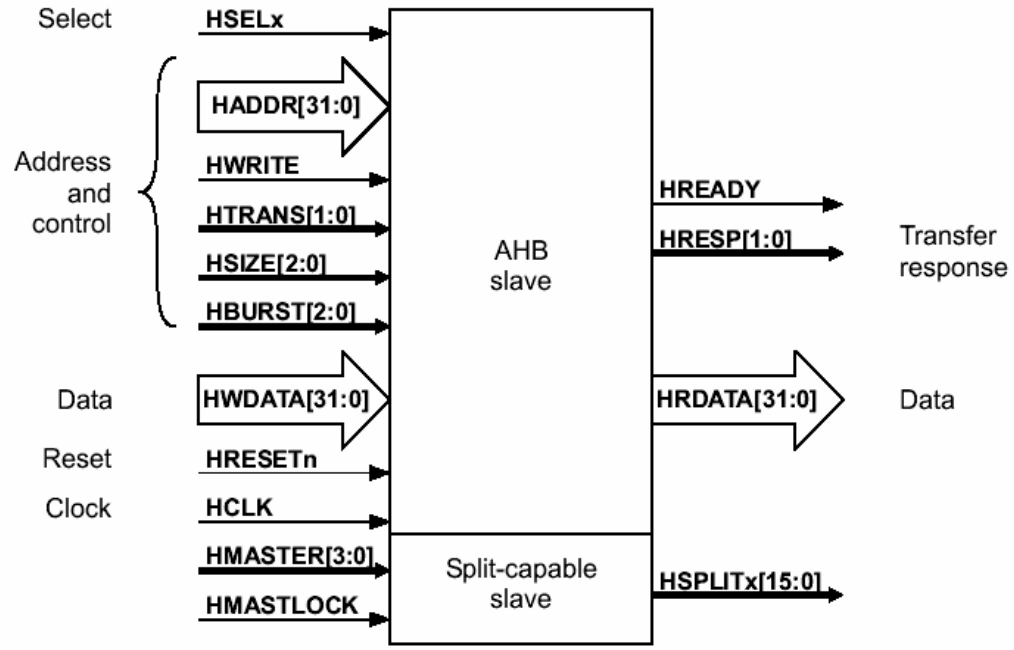

Fig. 4 AHB-Slave Interface Diagram

An AHB-Lite slave responds to transfers initiated by masters in the system. The slave uses the HSELx select signal from the decoder to control when it responds to a bus transfer.

The slave signals back to the master:

- The Success
- Failure
- Or Waiting for the Data transfer

IV.FINITE STATE MACHINE FOR AHB

Main component in the AMBA system is the master that can initiate the read or write transfer to any slave so it is imperative that master is properly designed for an AHB system to work. In addition AHB master implementation has to support advance features like burst transfers defined in the specification. So here in Fig 5 finite state machine is shown which support the features in the specification.

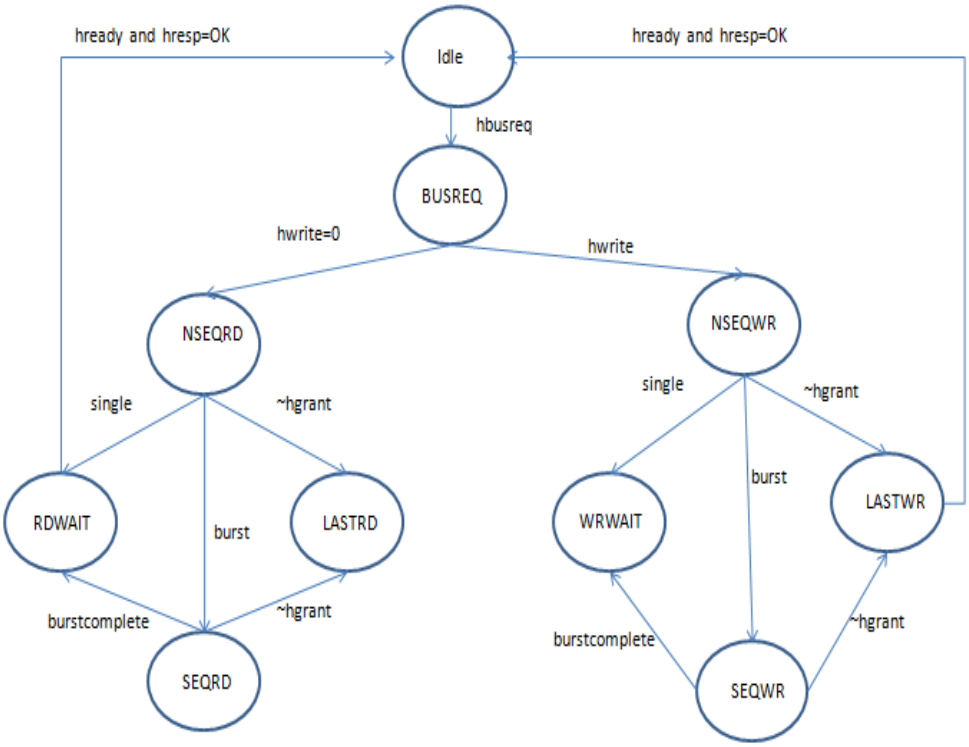

Fig.5 Finite State Machine of AHB

V. RESULTS

5.1 Input/Output for FSM of AHB

The input/output wave form for the Finite State Machine fig 5, is shown in fig 6.

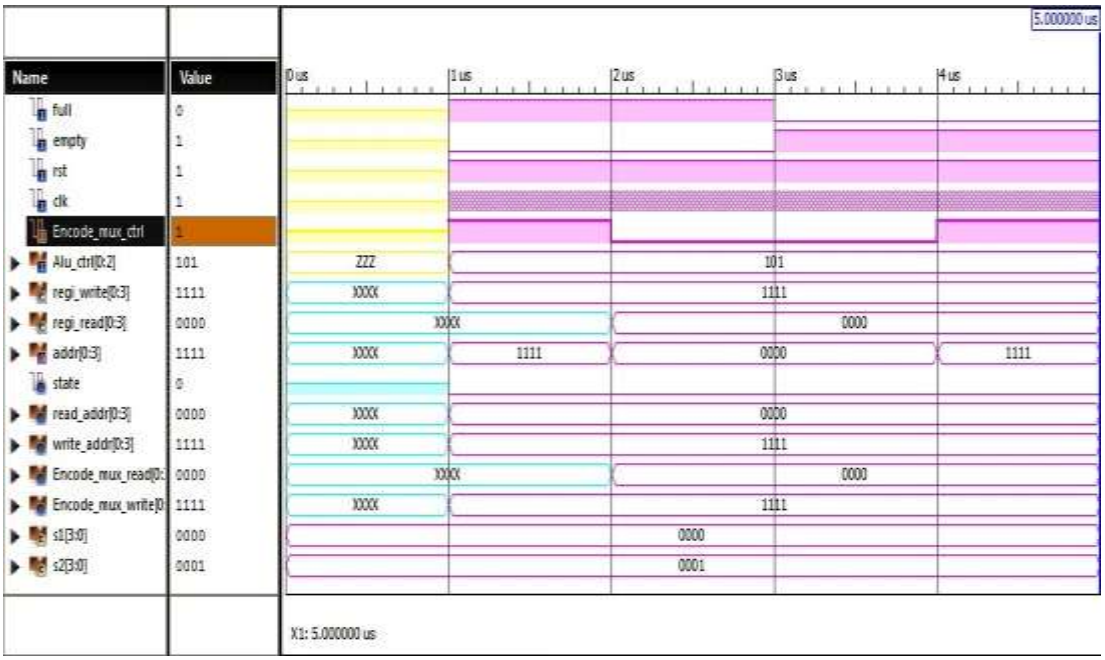

Fig.6 Output for FSM of AHB

After designing the finite state machine, any hardware description language is used to implement it and check it functionality for correctness. In this Project, the state machine is implemented in Verilog and Xilinx simulation tool is used to simulate the design and generate the waveforms.

5.2 FIFO Output

Fig 9 is the finalized simulated output wave form for the designed AHB using Split transaction method.

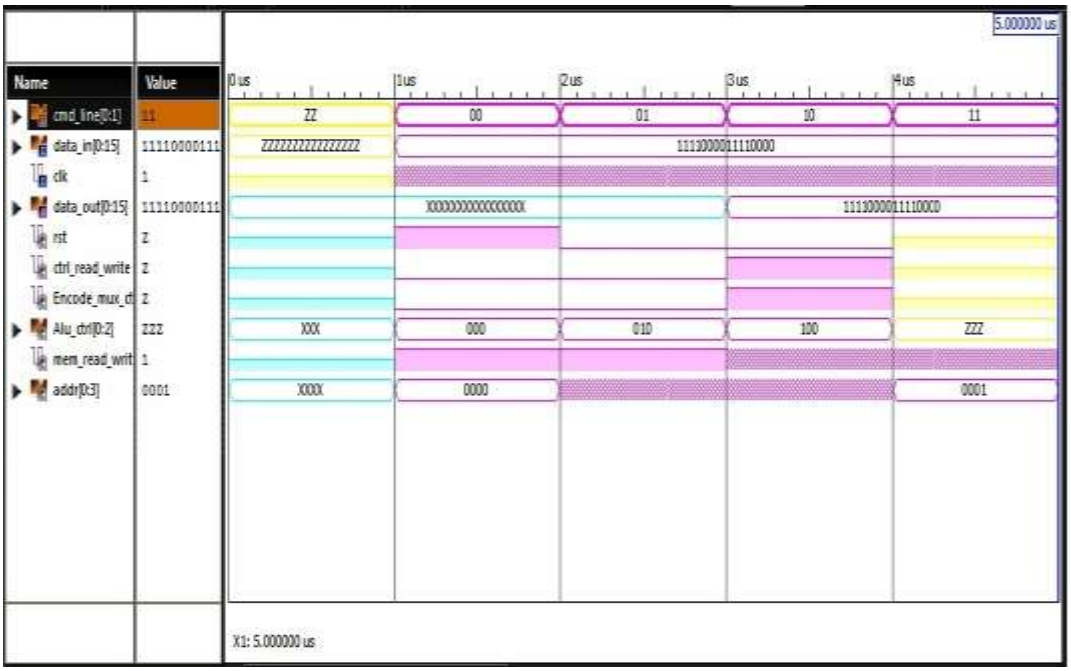

Fig 9 AHB FIFO Wave form

VI.CONCLUSION

In this paper the bit rate of Secured Digital Host Controller is increased by 2 Mbps using Split Transfer when compared to Burst Transfer. For a master that hands its request to interface, transaction is completed at the moment the request in handover to controller and bus is free. Thus not only the SDRAM memory is getting efficient but AHB bus utilization also enhances as per our design. The testing results shows 91.66% of reduced delay with FIFO when compared to the latency produced with FIFO, which is nothing but the in-built memory used within the SDRAM controller to improve its performance. In future, the algorithm used in the design of AHB Master Finite State Machine will be reconstructed in order to increase the bit rate upto the expected of 16 Mbps speed.

REFERENCES

[1] Pravin S. Shete, Dr. Shruthi Oza, "Design of an Efficient FSM for an Implementation of AMBA AHB Master", IJARCSEE volume 4, Issue 3, March 2014.

[2] Jaikiran l, Prakash biswagar, Theiventhiran Murugan, "Functional verification of Secured Digital Host Controller", IJESS, volume 3, Issue 1, 2013.

[3] Bhaumik Vaidya, Anupam Devani, "Design of an Efficient Finite State Machine for the Implementation of AMBA AHB Master", JIKRCE, volume 2, Issue 2, Nov 2013.

[4] Bhavana L. Mahajan, Ashiwale, Kshitija S. Patil, "Implementation of AHB protocol using FPGA", IJESAT, volume 2, Issue 4, Auguat 2012.

[5] Technical Committee SD Association. (2013): "SD Specifications Part A2 SD Host Controller Simplified - Specification Version 3.00". Retrieved February 25, 2013 from SD website: http://www.sdcard.org.

[6] Technical committee SD association. (2012): "SD Specifications Part 1Physical Layer Simplified Specification Version 3.01." Retrieved February 18, 2012 from SD website: http://www.sdcard.org.

[7] "AMBA Advanced High Performance Bus (AHB) Protocol specification". http://www.arm.com/

[8] Technical Committee SD Association. (2011): "SD Specifications Part 1 NFC (Near Field Communication) Interface Simplified Addendum Version 1.00". Retrieved November 08, 2011 from SD website: http://www.sdcard.org.

[9] AHB Example AMBA System. http://www.arm.com/

[10] "SD Specifications Part E1 SDIO Simplified Specification Version 3.00." February 25, 2011 from SD website: http://www.sdcard.org.