A NOVEL GENETIC ALGORITHM FOR SELECTIVE HARMONIC ELIMINATION IN CASCADE SWITCHED-DIODE MLC

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ABSTRACT

The multilevel inverters are robust and flexible in grid connected operations. This topology intelligently eliminates lower order harmonics such as 1, 3, 5, 7, 11 up to 19 by solving non-linear transcendental Fourier series equation. The conventional methods like Newton Raphson have problem of iterative and the initial guess are needed to solve non-linear equations. However the Genetic Algorithm eliminates the pre matured convergence as well as initial guesses. The new topology cascade switched diode MLC reduces the no of switches used in MI. Cascade switched-diode multilevel converter can produce many levels with minimum number of power electronic switches, gate driver circuits, power diodes, and dc voltage sources.

Key Words: Cascade, Harmonic Optimization, Multilevel Converter (MLC), Genetic Algorithm (GA).

1. INTRODUCTION

Multilevel inverters have drawn tremendous interest in high-power applications such as laminators, mills, conveyors, pumps, fans, blowers. Multilevel converters have been used for several applications such as static reactive power compensation, adjustable- speed drives, renewable energy sources. Multilevel converters can produce a large number of output voltage levels, which results in high voltage capability, better electromagnetic compatibility and high power quality. The principal function of multilevel converter is to synthesize a desired ac voltage from several separate dc sources. An attempt has been made in early for multilevel converter with reduced number of power electronic components in comparison with conventional cascade converter. This converter needs a large number of bidirectional switches. In addition, the magnitude of blocked voltage by bidirectional switches is high. In another new topology for cascade multilevel converter has been introduced, which reduces the number of bidirectional switches, power diodes, and dc voltage source in comparison with proposed topology. This topology consists of several sub multilevel converters and full-bridge converters. But, this topology requires a large number of bidirectional switches and gate driver circuit's .In this paper asymmetric, cascade switched-diode multilevel

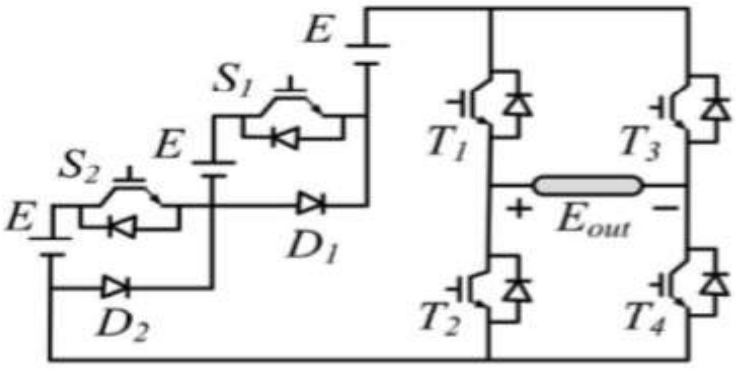
converter is used, which have more advantages in comparison with previous presented topologies. Many levels of voltage are produced with least number of components. The number of required power electronic switches against required voltage levels is a very important factor in designing of multilevel converter, because switches define the reliability, circuit size, cost, installation area, and control complexity. However increasing level produces harmonics. Switching strategies are applied to any inverters to control fundamental component and amount of produced harmonics. Mathematical methods are not suitable for high level inverters. Selective harmonic elimination pulse width modulation is the most famous switching strategy. The aim of this method is the eliminating low order harmonics, if it is possible, or at least to minimize them. The nature of these equations is nonlinear. Some iterative methods such as the Newton Raphson have been used to solve the equations .Iterative methods depend mainly on the initial guess and divergence problems are likely to occur. They have initial guesses and time of convergence is high. They are not used for high level inverters. They can only find one set of solutions. The GA is simple and applicable to problems with any number of levels, without the extensive derivation of analytical expressions, for both eliminating and minimizing harmonics. This algorithm is chosen for the optimization goals.

II CONSTRUCTIONAL FEATURE

Asymmetrical multilevel converter provides an increased number of output voltage levels for the same number of power electronic devices than its symmetric counterpart. To provide a large number of levels with less number of components, cascade switched-diode multilevel converters is used.. The output voltage of the proposed cascade switched- diode multilevel converter is given by

$$\mathbf{E_{out} = Eo1 + Eo2 + \cdots + Eon.}$$

The proposed asymmetric cascade topology for a seven level inverter.



The value of dc sources suggested as

E1 =E

E j =2 ^(j−1) E For j=2 ,3 ,4,...,Z.

For this method, the number of levels and maximum output voltage are given respectively

N level =2 (Z+1) −1

E_o max =(2Z −1)E

where Z represents the number of dc sources. In the proposed asymmetric topology, the number of IGBTs is obtained by

N_{IGBT} = Z +4

III CIRCUIT OPERATION

When the switch S is turned off, the current flows from the diode D and load voltage will be E. But, when the switch S is turned on, the diode is reverse biased and current flows from the voltage source E and load voltage will be (2E). By the use of this method, the load voltage is controlled. This method is the basic for this cascade multilevel converter.In this topology, the values of dc sources are unequal and voltages 50V, 50V, 10 V has been used in each cascade bridge.The output of 240v is obtained.In this topology, three dc sources and six IGBTs has been used. For the same number of levels, the symmetric CHB topology needs three dc sources and 12 IGBTs, which the number of IGBTs is higher than that of recommended symmetric structure.

It is obvious that increasing the number of level leads to the multilevel converter producing only near-sinusoidal output voltage waveform and, as a result, harmonic distortion. Therefore calculation of the optimal switching angles for the elimination of selected harmonics and reducing the total harmonic distortion must be done.

IV GENETIC ALGORITHM

This algorithm is usually used to reach a near global optimum solution. In each iteration of the GA a new set of strings, which are called chromosomes, with improved fitness is produced using genetic operators. A selection operator, a crossover operator which acts on a population of strings to perform the required reproduction and recombination, and a mutation operator which randomly alters character values, usually with a very low probability.They are generally solved by equating fourier equations to zero and then by obtaining switching angles.

Fourier series expansion for waveform is:

$$\mathbf{V\ (wt)} = \sum_{n=1}^{\infty} V_n \sin(wt)$$

where, V_n is the amplitude of the harmonics. The angles are limited to between zero and 90◦ ($0 \le \theta \le 90$). Because of an odd quarter-wave symmetric characteristic, the harmonics with an even order become zero. Subsequently, V_n becomes:

$$V_n = \begin{cases} 4V_{dc} \sum_{i=1}^{s} \cos(n\theta_i) & n: odd \\ 0 & n: even \end{cases}$$

For elimination of 5^{th} ,7^{th} harmonics, these three equations should be solved

$$M = [\cos(\theta_1) + \cos(\theta_2) + ..+ \cos(\theta_4)]/4$$

$$0 = [\cos(5\theta_1) + \cos(5\theta_2) + \ldots + \cos(5\theta_4)]$$

$$0 = [\cos(7\theta_1) + \cos(7\theta_2) + ..+ \cos(7\theta_4)]$$

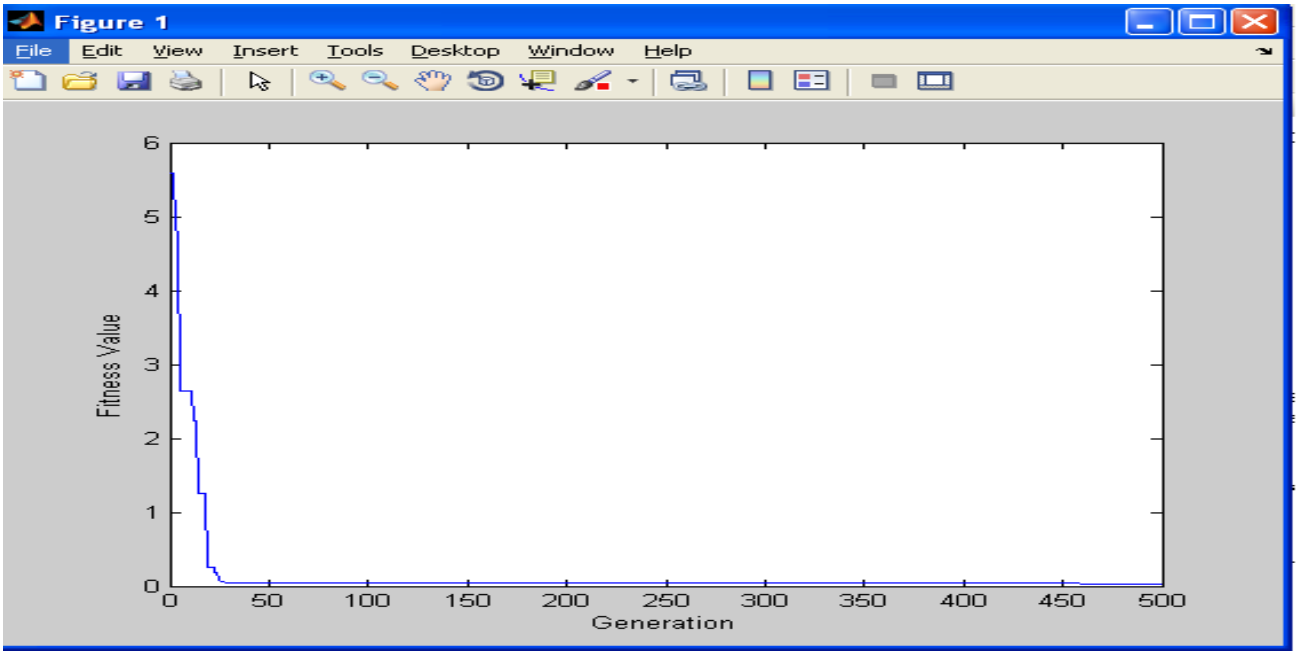
The modulation index is given by

$$M \triangleq V1 \Big/ \frac{4V_{dc}S}{\pi}$$

The value of M is between 0 and 1 to cover different values of V_1. It is necessary to determine switching angles, namely θ1, θ2, θ3 such that the equation sets are satisfied.

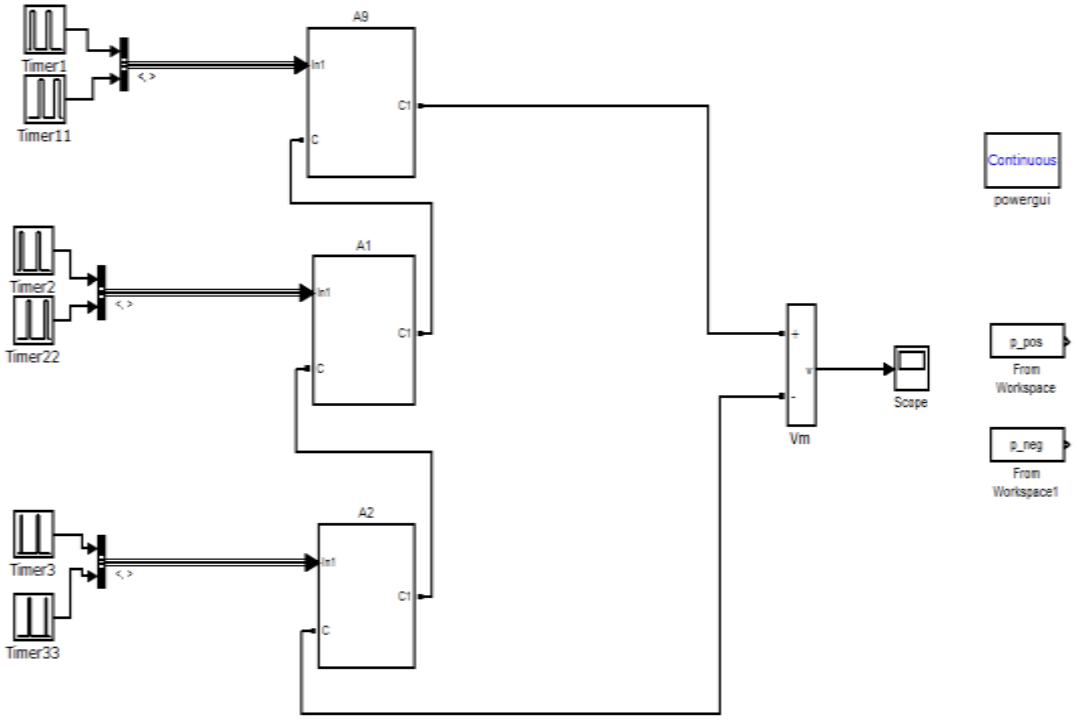
The output of genetic algorithm is switching angles corresponding to level and modulation index. The coding can be done for n levels. The output of GA is given to multilevel inverter as input.

The output graph for GA representing genereation against fitness value

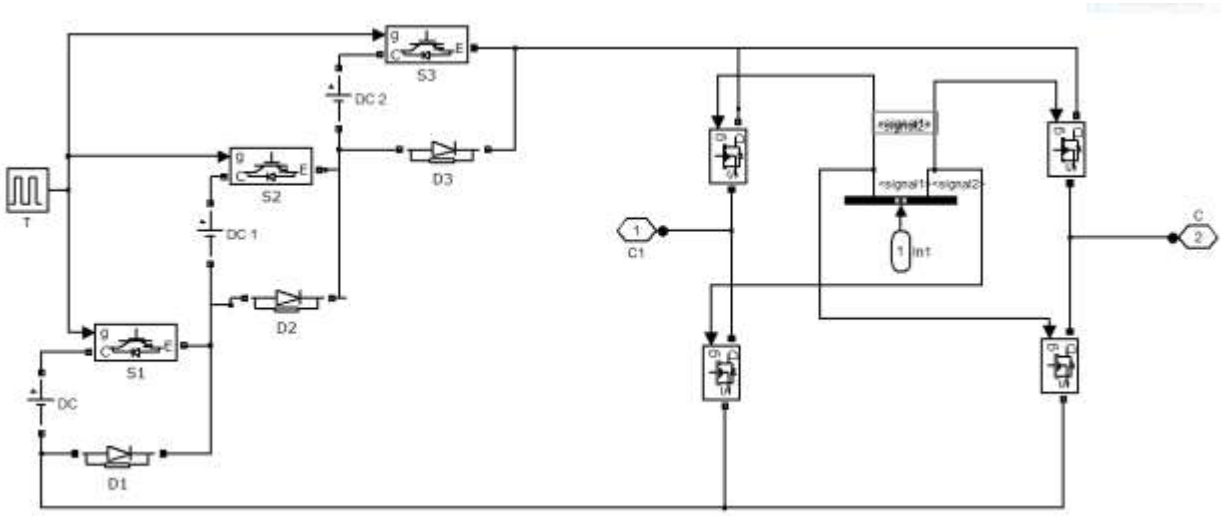


V PROPOSED MODEL

The simulation model for proposed seven level system is

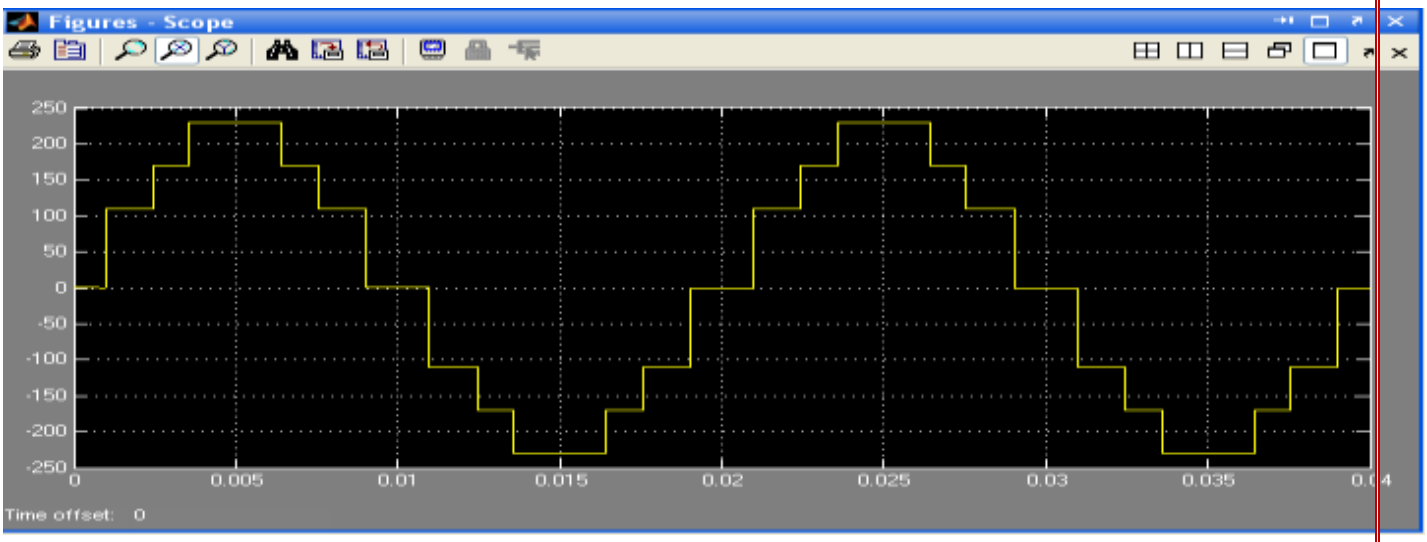


The subsystem for single cascade switched diode bridge is

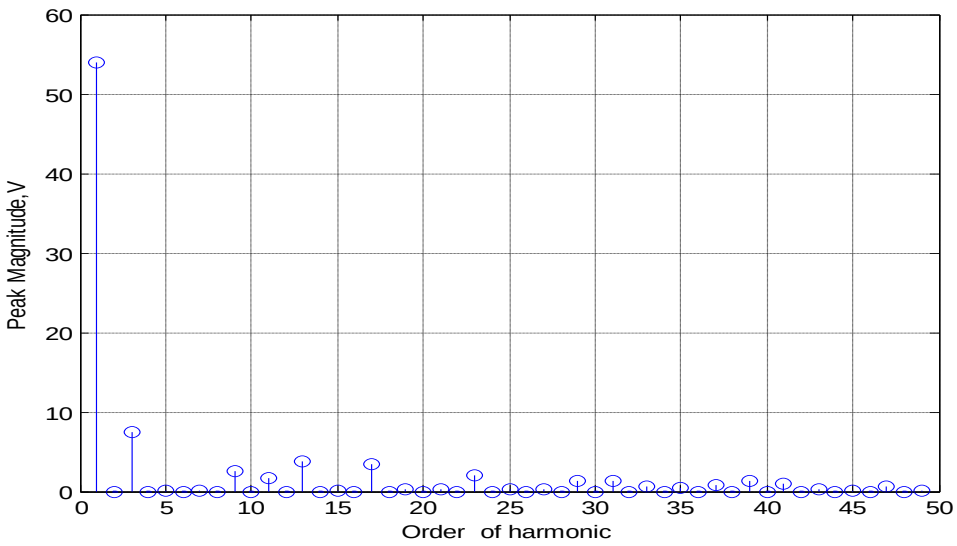


VI STIMULATION RESULTS

The simulation output for cascade seven level inverter is given below



The lower order harmonics are eliminated using genetic algorithm. Reduced harmonic output graph can be obtained. The harmonic order corresponding to peak order graph is given below



VII CONCLUSION

The cascade structure extends the design flexibility and the possibilities to optimize the converter for different objectives such as minimization of number of IGBT's, gate driver circuits, dc voltage sources, standing voltage on switches and power diodes. Less number of components leads to the reduction of size, simple control strategy and high efficiency. Harmonics caused by increasing levels are optimized using genetic algorithm by eliminating lower order harmonics. GA is better for optimizing THD in multilevel converters.

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