EFFICIENT LAYOUT OF FREDKIN GATE WITH MINIMIZED AREA

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ABSTRACT

Quantum cellular automata (QCA) is a new technology in nanometre scale (<18nm) to support nano technology. QCA is very effective in terms of high space density and power dissipation and will be playing a major role in the development of the Quantum computer with low power consumption and high speed. This paper describes the design and layout of a fredkin gate based on quantum-dot cellular automata (QCA) using the QCADesigner design tool. The fredkin design is based on combinational circuits which reduces the required hard-ware complexity and allows for reasonable simulation times. The paper aims to provide evidence that QCA has potential applications in future Quantum computers, provided that the underlying technology is made feasible. Design has been made using certain combinational circuits by using Majority gate, AND, OR, NOT in QCA. The QCA is a novel tool to realize Nano level digital devices and study and analyze their various parameters.

Keywords: Fredkin Gate, Nano-Technology, QCA

I. INTRODUCTION

Quantum Dot cellular automata (QCA) is an emerging technology that takes advantage of quantumeffects, which become increasingly apparent at the scale of a few nanometers. Previous work has shown that QCA has several novel features not available with conventional FET-based circuits [1]. Although the design cost function is different from FETbased technologies [2], a significant effort has already been started into exploring alternative arithmetic architectures that are portable to QCA, such as systolic arrays and bit-serial circuits. Recently, several successful studies into computer arithmetic and memory structures have provided further motivation for research into the realization of QCA technology [2-8]The QCA cell [9] consists of a system of four quantum dots charged with only two free electrons. Electrostatic repulsion between these electrons force them to occupy only the diagonal sites creating a so called "polarization" used to encode binary information, as seen in Figure 1. Interactions between neighboring cells allow for the layout of functional circuits, where the objective is to layout the cells in such a way that the ground state polarization of the output cells represents the correct output of a function to a given set of input vectors. The software simulation tool used for the realization of this technology is QCADesigner [15] by Walus group at university of British Colombia.

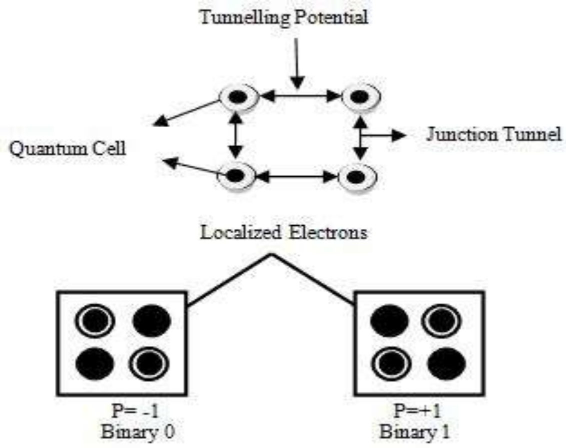


Fig:1 QCA Cell Polarization

To date, proof of concept QCA cells have been experimentally verified using a device which exploits the Coulomb blockade phenomenon [10], although the originally proposed cell is still beyond present fabrication capabilities. As a result, investigators are currently looking at creating QCA cells using single molecules [11].At first, it may appear premature to begin in depth investigation into the design of large circuits such as the one proposed here prior to the realization of a final technology. However, due to the capabilities of today's computers, the cost of such investigations is relatively low when compared to experimental studies. Such investigations provide a feedback mechanism in the development loop that can fairly rapidly include or exclude new device implementation concepts based on their potential application in these larger circuits. Using simulations we have, for example, identified a fundamental requirement for multilayer capability in complex circuits, previously believe unnecessary [12]. The physical interactions between cells may be used to realize elementary Boolean logic functions. The basic logic gates in QCA are the Majority logic function and the Inverter. The Majority logic function can be realized by only 5 QCA cells. The logic AND function can be implemented from a Majority logic function by setting one input permanently to 0 and the logic OR function can be Implemented from a Majority logic function by setting one input permanently to 1.Each gate is made to perform each performance Based on the mutual interaction between cells, basic logic components including an inverter and a three-input majority gate can be built in QCA. An inverter is made by positioning cells diagonally from one another to achieve the inversion functionality. A majority gate consists of five QCA cells that realize the following function:

M(a,b,c)=ab+bc+ca-------------------→(a)

Majority gates can be easily converted to AND or OR gates by using a fixed value for one of the

inputs. For example, a two-input AND gate is realized by fixing one of the majority gate inputs to "0":

AND(a,b)=M(a,b,0)=ab-------------------→(b)

Similarly, an OR gate is realized by fixing one input to "1":

$OR(a,b)=M(a,b,1)=a+b$ --------------------→©

In combination with inverters, these two logic components can be used to implement any logic function.

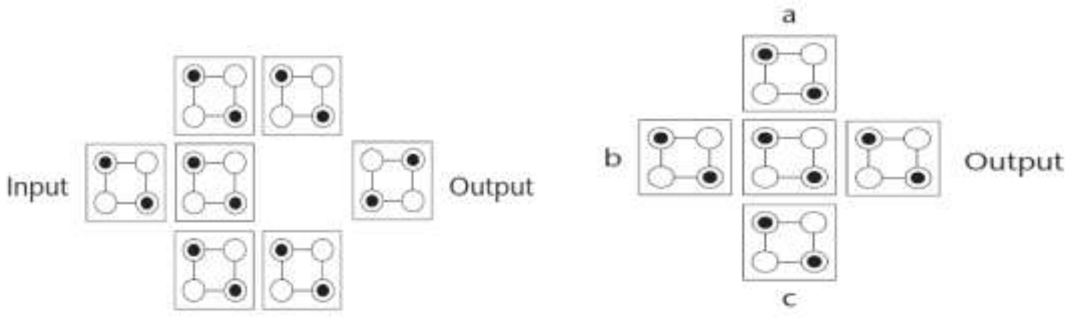


Fig 2QCA basic gates:(a) inverter, (b) majority gate.

II. CONSERVATIVE REVERSIBLE FREDKIN GATE

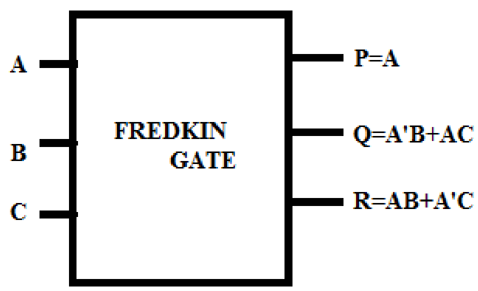


Fig 3 Fredkin gate

In fredkin gate we can perform different logic functions such as buffer,NOT,AND andOR.Along with fredkin gate many researchers invented the toffli gate and feymanngate.But as a result and conclusion from the three gate,the fredkin gate contains the minimum garbage outputs.Following figures and description is discussing about Fredkin gate and its benefitThe above fig 3 shows the block diagram of fredkin gate,the inputs are A,B,C and outputs are P,Q,R..It contains two OR gate and four AND gate.Inexisiting method[1] they used to implement the fredkin gate with cross wires,more majority gates and long array wires

III. BACKGROUND AND RELATED WORK

A number of different implementations to realize the bistable and local interaction required by the QCA paradigm have been proposed. Both electrostatic interaction-based QCA implementations (metal-dot, semiconductor, and molecular) and magnetic QCAs have been investigated.

Metal-Island QCA

The metal-island QCA cell was implemented with relatively large metal islands (about 1 micrometer in dimension) to demonstrate the concept of QCA [13, 16]. The dots are made of aluminum with aluminum oxide tunnel junctions between them. In this metal-island QCA cell, electrons can tunnel between dots via the tunnel junctions. These two pairs of dots are coupled to each other by capacitors. Two mobile electrons in the cell tend to occupy antipodal dots due to electrostatic repulsion.

Semiconductor QCA

A semiconductor QCA cell is composed of four quantum dots manufactured from standard semi conductive materials [20–22]. A device was fabricated in [23] using a GaAs/AlGaAs hetero structure with a high-mobility two-dimensional electron gas below the surface. Four dots are defined by means of metallic surface gates. The cell consists of two double Quantum-Dot systems (half cells).Half cells are capacitively coupled. The charge position is used to represent binary information

Molecular QCA

A molecular QCA cell [25–28] is built out of a single molecule, in which charge is localized on specific sites and can tunnel between those sites. In the molecule shown in [29], the free electrons are induced to switch between four ferrocene groups that act as quantum dots due to electrostatic interactions, and a cobalt group in the center of the square provides a bridging ligand that acts as a tunneling path.

Magnetic QCA

A magnetic QCA cell is an elongated nanomagnet with a length of around 100 nm and a thickness of 10 nm. The shape of the nanomagnet varies for different schemes. The binary information in magnetic QCA cells is based on their single domain magnetic dipolemoments. The usage of magnetic interaction inherently minimizes the energy.

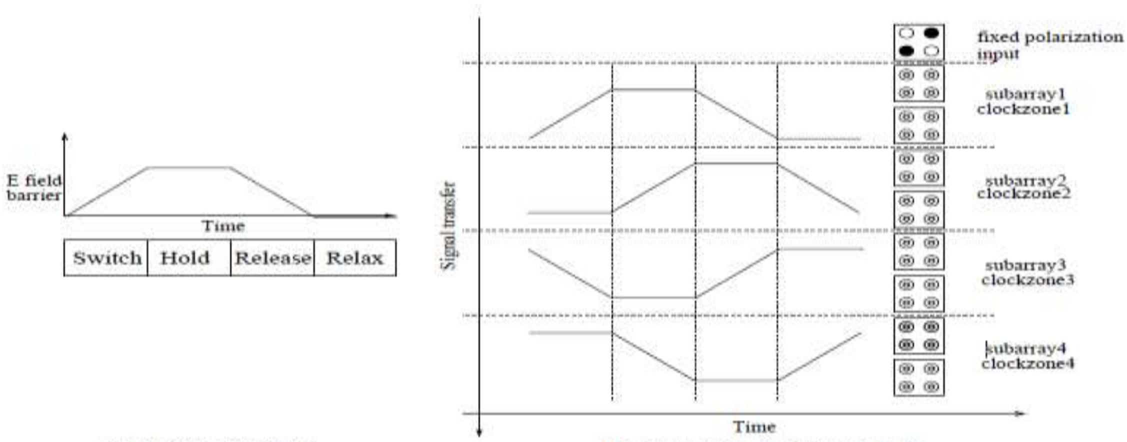
3.1 Related Work

The testing of QCA was addressed for the first time in a seminal work reported in [4], where the defect characterization of QCA devices was investigated, and it was shown how the testing of QCA was different from conventional CMOS. The modeling of QCA defects at molecular level was done for combinational circuits in [11]. Fault characterization was done for single missing/additional cell defect on different QCA devices such asMV, INV, fan-out, crosswire, and L-shape wire. The test generation framework for QCA was presented in [10]. It was shown that additional test vectors can be generated for detecting QCA defects that remain undetected by the stuck-at fault model. Bridging fault on QCA wires was also addressed.

Clocking

In VLSI systems, timing is controlled through a reference signal (i.e., a clock) and is mostly required for sequential circuits. Timing in QCA is accomplished by clocking in four distinct and periodic phases and is needed for both combinational and sequential circuits. Clocking provides not only control of information flow but also true power gain in QCA. Signal energy lost to the environment is restored by the clock.

Two Types Of Switching Methods: Abrupt switching and adiabatic switching. In abrupt switching, the inputs to the QCA circuit change suddenly and the circuit can be in some excited state; subsequently, the QCA circuit is relaxed to ground state by dissipating energy to the environment. This inelastic relaxation is uncontrolled and the QCA circuit may enter a metastable state that is determined by a local, rather than a global energy ground state. Therefore, adiabatic switching is usually preferred; in adiabatic switching, the system is always kept in its instantaneous ground state. A clock signal is introduced to ensure adiabatic switching.



(a) 4 Phase Clocking (b) Switching of a Binary Wire

For QCA, the clock signals are generated through an electric field, which is applied to the cells to either raise or lower the tunneling barrier between dots within a QCA cell. This electric field can be supplied by CMOS wires, or CNTs buried under the QCA circuitry. When the barrier is low, the cells are in a non-polarized state; when the barrier is high, the cells are not allowed to change state. Adiabatic switching is achieved by lowering the barrier, removing the previous input, applying the current input and then raising the barrier. If transitions are gradual, the QCA system will remain close to the ground state.

The clocked QCA circuit utilizes the tri-state six-dot cells, as shown in Fig 5. The clock signal is applied to either push the electrons to the four corner dots or pull them into the two middle dots. When the electrons are in the middle dots, the cell is in the “null” state. When the electrons are in the four corner dots, the cell is in an active state. The charge configuration of the cell in active state represents binary “0” and “1” as shown previously in Figure 1. A molecule with three quantum-dot hole sites is shown in Figure 2. Two such molecules form a six-dot QCA cell

This Clocking Scheme Consists Of Four Phases

Switch, Hold, Release and Relax, as shown in Figure 4.. The QCA circuit is partitioned into so-called clocking zones, such that all cells in a zone are controlled by the same clock signal. Cells in each zone perform a specific calculation. During the Relax phase, the electrons are pulled into the middle dots, so the cell is in “null” state. During the Switch phase, the inter dot barrier is slowly raised and pushes the electrons into the corner dots, so the cell attains a definitive polarity under the influence of its neighbors (which are in the Hold phase). In the Hold phase, barriers are high and a cell retains its polarity and acts as input to the neighboring cells.

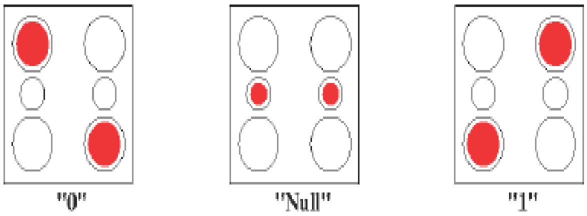


Fig 5 Schematic Diagram of a Six-dot QCA Cell

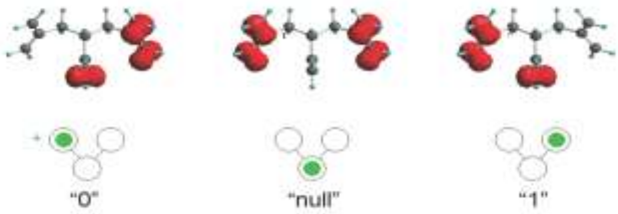


Fig 6Tri-state Quantum-dot Molecule

Finally in the Release phase, barriers are lowered and the electrons are pulled into the middle dots so the cell loses its polarity. Here switching is adiabatic, i.e. the system remains very close to the energy ground state during transition, and the stationary state of each cell can be obtained by solving the time-independent Schrodinger equation. Clocking zones of a QCA circuit or system are arranged in this periodic fashion, such that zones in the Hold phase are followed by zones in the Switch, Release and Relax phases. A signal is effectively "latched" when one clocking zone goes into the Hold phase and acts as input to the subsequent zone.In a clocked QCA circuit, information is transferred and processed in a pipelined fashion and allows multi-bit information transfer for QCA through signal latching. All cells within the same zone are allowed to switch simultaneously, while cells in different zones are isolated. initially, subarray1 switches according to the fixed input, and subarray2 shows no definite polarization at this time. Then, subarray1 enters the Hold phase; at this time subarray2 starts switching. As subarray3 is in the relaxed state, it will not influence the computational state of subarray2. Next, subarray1 is moved to a Release phase; subarray2 is in the Hold state and serves as the input to subarray3 (which is in the switch phase). The signal is "latched" when subarray1 enters the Hold phase and acts as input to subarray2.In the adiabatic switching schemes, fluctuations in operating temperature T may excite QCA cells above their ground state and produce erroneous results at the output. An analysis of these thermal effects on a line of N QCA cells is provided in . It has been shown in [1] that for reliable kink-free computation, within a single clocking zone, N is bound by e EkkBT . Large QCA circuits are therefore partitioned into smaller sub circuits, each of which resides in its own clocking zone. The clock signal is commonly generated by CMOS wires buried under the QCA circuitry. Fig 6 depicts the schematic diagram for clocking a 3-dot molecular QCA array [28]. QCA molecules are located in the xz plane and clock wires are placed in the z direction, thus inducing an electrical field in the y direction. One of the limiting factors for high density of QCA systems is the wiring requirements for the generation of the electrical field. The use of single walled carbon nanotubes (SWNTs) and a new clock wire layout is recommended in [31].

It has been shown that metallic SWNTs are excellent conductors [34] and can be used to generate a clocking field that smoothly propagates the QCA signals. The layout method of [35] consists of a series of clocking wires perpendicular to the QCA signal direction.In this method, the direction of the perpendicular clocking wires must be changed with turns in the QCA signals. The approach proposed in [31] allocates clocking wires at a 45o angle .hence, only two clocking directions are needed to allow QCA signal propagating along the two axes.

IV.QCA SIMULATORS

Several QCA simulators are currently available, They are mAQUINAS and QCADesigner are physics-based and solve quantum equations for Quantum-Dot Cellular Automata cell interactions. mAQUINAS assumes a continuous clocking scheme envisioned for the molecular QCA systems. Adiabatic switching is assumed where the system is kept close to the ground state. At each time step, the time independent Schrodinger equation is solved for each cell. The process continues until a self consistent solution is found for the entire system. QCADesigner [27] has been used to produce results presented in the book, and will be discussed in more detail next. However, quantum simulation is computation intensive and are not suitable for large circuits. QBert is another simulator developed for digital logic simulation for QCA which can be run much faster. A new model based on a SPICE model has been proposed and experimentally verified.

V.SIMULATIONS AND RESULTS

In existing fredkin gate they used to design the fredkin gate with Binary wires,cross wires and 6 Majority Voters.But in this paper describes about Fredkin gate implement with minimum area that contain only Binary wires and 4 Majority voters. Existing paper produced fredkin gate using 246 cells in QCA Designer tool.In this paper the fredkin gate implemented using 133 cells only,so the implementation area will be minimizes.

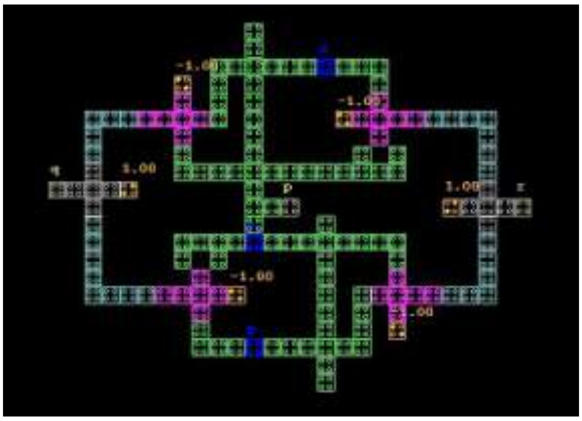


Fig 7 Proposed layout of fredkin gate

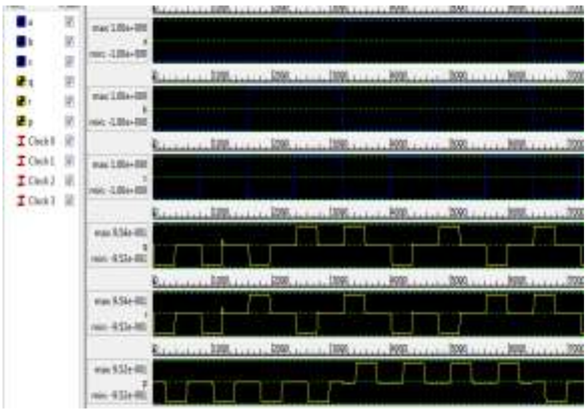


Fig 8 Output waveform

Table1Truthtable

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Existing fredkin gate	246	4s
Modified fredkin gate	133	1s

Table 2 Comparison Table of fredkin

S.no	GATES NAME	NO.OF.CELLS	KINK ENERGY	POLARIZATION	SIMULATION TIME
1	INV	11	$14.44*10^{-21}$	e^{001} ±9.54	0
2	OR	5	$22.09*10^{-21}$	e^{001} ±9.54	0
3	AND	5	$19.43*10^{-21}$	e^{001} ±9.54	0
4	MODIFIED FREDKIN	133	$150.78*10^{-21}$	e^{001} ±9.54	1s

gate7 shows the existing and proposed fredkin gate layout.Abovetable prescribes the truth table for fredkin gate.The inputs are A,B,C and Outputs are P,Q,R.The output of P displays the input of A,Hence we can understood that fredkin gate implement as buffershows the output waveform of fredkin gate, and it was simulated in bistableengine.The option parameters for fredkin gate of bistable engine is given below.

5.1 Equation

- Electrostatics interactions between the electrons in QCA is

$$E=\frac{Q1\,Q2}{4\pi\varepsilon_0\varepsilon_r r}$$

The interaction is determines the kinetic energy between two cells, thus the kinetic energy is

$$E_{kink}=E_{opp.pol}-E_{same\ pol}$$

From this equation we can calculate the kink energy of fredkin gate and others.The table for kink energy is shown below.In table 3 contains the calculation result from kink energy equation.Table2 contain the comparison between the existing and Proposed fredkin gate layout

VI.CONCLUSION

Each gate is made to perform each performance,But in fredkin gate we can perform different logic functions such as buffer,NOT,AND and OR. Along with fredkin gate many researchers invented the toffli gate and feymanngate.But as a result and conclusion from the three gate,the fredkin gate contains the minimum garbage outputs. In existing fredkin gate they used to design the fredkin gate with Binary wires,cross wires and 6 Majority Voters.But in this paper describes about Fredkin gate implement with minimum area that contain only Binary wires and 4 Majority voters. Existing paper produced fredkin gate using 246 cells in QCADesignertool.In this paper the fredkin gate implemented using 133 cells only,so the implementation area will be minimizes.Here I conclude that my fredkin gate design consumes low power dissipation,Area and delay.

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