



# REVIEW OF DETERMINISTIC ROUTING ALGORITHM FOR NETWORK-ON-CHIP

Garba Adamu<sup>1</sup>, Mr. Pankaj Chejara<sup>2</sup>, Dr. Ahmed Baita Garko<sup>3</sup>

<sup>1,2</sup>Department of Computer Science, Sharda University, (India)

<sup>3</sup>Department of Computer Science, Federal University Dutse, Nigeria

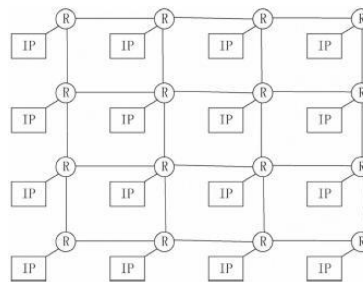
## ABSTRACT

Network-on-chip (NoC) has been introduced as a new paradigm to solve System on chip (SOC) design challenges. The Network-on-Chip (NoC) architecture is a viable solution to the complex on-chip communication problems. Communication performance of NOC's is heavily depends on routing algorithm. The architecture of NOC is based on topology, routing algorithm and switching techniques. The routing algorithm is one of key ingredient in NOC architecture. A routing algorithm determines how the data is routed from source router to destination router. The routing algorithms are classified base on their key characteristics. The classification is either where routing decision is taking or a path the packet follows. This paper presents review of deterministic routing algorithm in details, it advantage and disadvantage.

**Keywords:** *Deterministic Routing Algorithm, Deterministic XY Routing, DOR, Network-On-Chip And Pseudo Adaptive Routing*

## I. INTRODUCTION

As the technology continues to improve, memories and processors are becoming inexpensive with increase speed, the problem of communication in the processors arises, because traditional buses cannot meet the requirement especially in large system scalability and difficulties in single clock synchronization, other limitations like high propagation delay, latency and power consumption make buses unattractive. Network-on-chip (NoC) is the new paradigm where traditional buses are replace with small router that are connected to each other between endpoints in the processors, NoC helps in reducing power consumption, area size and propagation delay in the processors and NOC employs the concept of computer network the only difference is that in NOC traffic is analyse during design period, and the traffic is spread among the node to avoid congestion [1]. Understanding routing algorithm is critical in the design process of any NoC architecture. Previous work was done on different types of XY routing algorithm and its use on different network conditions. Others consideration of the previous work was application and traffic condition of the various XY routing algorithm.



**Figure 1.0 4×4 of 2D Mesh Topology**

The routing algorithm is key factor which affects NOC network communication. This paper will discuss routing algorithm and review deterministic routing algorithm which is simple to use in any NoC architecture.

## II. OVERVIEW OF NOC DESIGN APPROACH

The design of Network-on-chip (NoC) is based on Switching technique, Topology and Routing algorithm

### 2.1 Switching Technique

There are two major switching techniques: circuit switching and packet switching. Circuit switching establishes a link between source and destination node either virtually or physically before a message is being transferred [2]. Major advantages of circuit switching are that there is no contention delay during message transmission and its behavior is more predictable. In packet switching, messages are divided into packets at the source node and then sent into a network. Packets move along a route determined by the routing algorithm and traverse through a series of network nodes and finally arrive at the destination node [2]. Packet switching is utilized in most of NoC platforms because of its potential for providing simultaneous data communication between many source-destination pairs. Packet switched networks can further be classified as Wormhole, Store and Forward (S&F), and Virtual Cut Through Switching (VCT) networks [2]. In Wormhole switching networks, only the header flit experiences latency. Other flits belonging to the same packet simply follow the path taken by the header flit. If the header flit is blocked then the entire packet is blocked. It does not require any buffering of the packet. Therefore, the size of the chip drastically reduces.

### 2.2 Topology

Topology is a very important feature in the design of NoC because design of a router depends upon it. Network topology determines the number of router to be connected, their channels and how are connected [3]. Different topologies are proposed for the design of NoC.

#### 2.2.1 Mesh

Mesh topology is favored by many research groups because of its layout efficiency. It has good electrical property and can address the on-chip resources in a simple manner. A mesh-shaped network consists of  $m$  columns and  $n$  rows [4]. The routers are situated in the intersections of the two wires and the computational resources are near routers.

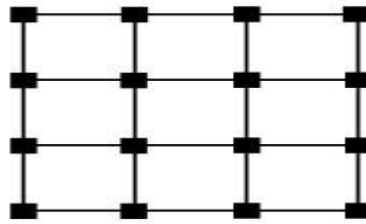


Figure 2.2.1 Mesh Topology

### 2.2.2 Torus

A Torus network is an improved version of basic mesh network. A simple torus network is a mesh in which the heads of the columns are connected to the tails of the columns and the left sides of the rows are connected to the right sides of the rows [4]. The path diversity of torus is better than the mesh network, and it also has more minimal routes.

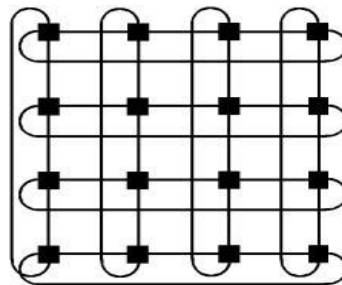


Figure 2.2.2 Torus Topology

### 2.2.3 Tree

In a tree topology nodes are routers and leaves are computational resources. The routers above a leaf are called as leaf's ancestors and correspondingly the leaves below the ancestor are its children [4].

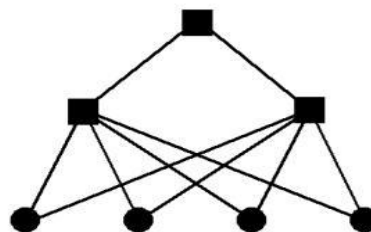


Figure 2.2.3 Tree Topology

### 2.2.4 Butterfly

A butterfly network is uni- or bidirectional and butterfly-shaped network typically uses a deterministic routing. Packets arriving to the inputs on the left side of the network are routed to the correct output on the right side of the network [5].

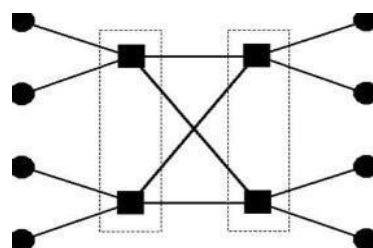


Figure 2.2.4 Mesh Topology



### **2.3 Routing Algorithm in Network-on-Chip**

Routing algorithms are used to determine the sequence of channels a message packet traverses from the source to the destination. In other words, routing algorithm determine which path a packet will takes from source router to destination router [6].

Different types of routing algorithm exist in NOC, which are differentiated according to their key characteristics:

If we consider the place where routing decision is made they may be grouped as centralized, source and distributed routing algorithm. If an algorithm is centralized the path is chosen by a central controller, if it is source the path is chosen by a source router prior to a sending the packet, if it is distributed the path is chosen by an intermediary routers [7].

If we consider how to choose a path routing algorithm are classified as deterministic and adaptive algorithm.

Deterministic algorithm does not take into account the network condition before choosing a path from source to destination.

In adaptive algorithm network load, traffic condition and information about available output channel are always taken into consideration.

In this paper deterministic routing algorithm is explore in details and where it is use in NOC. As explained earlier, deterministic routing algorithm route packet every time from point A to another point B along a fixed path without considering network condition [8]. In congestion free network deterministic routing algorithm are reliable and have low latency. All real time system use deterministic algorithm because packet reach destination in correct order and so reordering is not necessary. Deterministic routing algorithms are greedy algorithm because they always choose shortest path from source to destination [6].

The drawback of deterministic routing algorithm is that network condition is not consider, therefore, if the network is congested and another packet is send the whole network will fail.

### **2.4 Types of Deterministic Routing Algorithm**

**2.4.1 Dimension-order-routing (DOR)** algorithm is considered to be one of the most popular deterministic routing algorithms due to its simplicity for implementation and good performance according to average packet delay and throughput metrics. The algorithm determines to what direction packet are routed during every stage of the routing [6].

#### **2.4.2 XY Routing Algorithm**

XY routing is a dimension order routing which routes packets first in x- or horizontal direction to the correct column and then in y- or vertical direction to the receiver. XY routing suits well on a network using mesh or torus topology. Addresses of the routers are their xy-coordinates.

There are some problems in the traditional XY routing. The traffic does not extend regularly over the whole network because the algorithm causes the biggest load in the middle of the network. There is a need for algorithms which equalize the traffic load over the whole network.

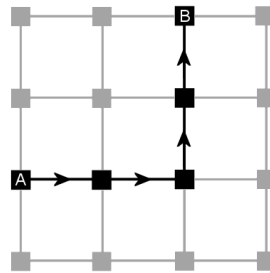


Figure 2.4.2 XY Routing Algorithm

**2.4.3 Pseudo Adaptive XY Routing:** Pseudo adaptive XY routing works in deterministic or adaptive mode depending on the state of the network. The algorithm works in deterministic mode when the network is not or only slightly congested. When network becomes blocked, the algorithm switches to the adaptive mode and starts to search routes that are not congested [6].

### III. CONCLUSION

In this paper, we introduce the concept of network-on-chip as new paradigm that replaces system-on-chip (SoC), the important design parameter to consider when designing network on chip: switching technique, topology and routing algorithm. We explain the various classification of routing algorithm and their characteristics. Deterministic routing algorithm as a simplex form of algorithm in network-on-chip due to hardware simplicity, low latency and simple routing logic, mostly all real time system use this routing algorithm because packet reach destination in correct order and reordering is not necessary. Deterministic routing is a greedy algorithm because it always chooses a shortest path to deliver a packet from source to destination.

### REFERENCES

- [1] Abelardo Jara, J. Bevis, and A. Sanchez Network-on-Chip: A Quick Introduction March, 2009
- [2] Anurahda K. Shrimawale and Mahendra A. Gaikwad Review of odd-even routing algorithm for 2D mesh topology of network-on-chip architecture for busy traffic, International journal of computer application (0975 – 8887). Recent trend in engineering technology – 2013
- [3] Shubhangi DChawade, Mahendra A Gaikwad and Rajendra M Patriker Review of XY routing algorithm for Network-on-Chip architecture, International journal of computer application (0975 – 887) Volume 43 – No 21 April, 2012
- [4] N. Ashokkumar, P Nagarajan and S Ravanaja Survey Exploration of Network-on-Chip Architecture
- [5] Maksat Atagoziyev Routing algorithm for on chip network, master dissertation Middle East Technical University 2007 (p7 – 13)
- [6] Ville Rantala, Teijo Lehtonen and Juha Plosila Network-on- Chip routing algorithm TUC technical report No. 779 August, 2006
- [7] Jayant Kumar Singh Performance evaluation of different routing algorithm in network on chip master dissertation National Institute of Technology Rourkella, Odisha

- [8] Shuyan Tiang, Shanshan Jiang, Peng Liu, Yue Liu and He Chang Network-on-chip base tolerant routing algorithm and implementation, transaction of computer science & technology volume 2, Issue 4 December 2013