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DESIGN OF DCT ARCHITECTURE USING ARAI ALGORITHMS

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ABSTRACT

*Nowadays the demand for applications capable of high dynamic range(HDR) video is increasingly widely. Such high dynamic range (HDR) video systems operating at high resolution require an associate hardware capable of significant throughput all allowable area & complexity. The circuit realization of the Discrete Cosine Transform (DCT) is compatible with noise, distortion, circuit area, power consumption of the related video devices[1]. The 8*8 Discrete Cosine Transform (DCT) is popularly used for video & image compression, which is a core component in contemporary media standards such as JPEG & MPEG. The main reason for the widespread adaptation of the DCT are its favourable properties called decorrelation, energy compaction, separability, symmetry, and orthogonality[2]. The energy compaction properties of the DCT is very much close to the Karhunen transform, which is of much higher computational complexity due to requirements for numerical optimization. There are many algorithms that are proposed to reduce the hardware complexity of DCT computation by exploiting properties of the transform. Hence the Arai Algorithm is used due to its low computational complexity.*

All implementations are functional on a Xilinx Virtex-7 XC7V285T FPGA device.

Keywords: Arai; Discrete Cosine Transform (DCT); FPGA Designs.

I. INTRODUCTION

Compression is nothing but the process of reducing the size of the data sent as well as necessary bandwidth required for the digital representation of a signal. There are two categories of compression: Lossy compression and lossless compression.

The Scheme Discrete Cosine Transform (DCT) on which we are working is a lossy compression scheme in which image block of N*N is transformed from the spatial domain to the DCT domain[2]. In DCT the lower frequency DCT coefficients will appear towards the upper left-hand corner and the higher frequency coefficients are in the lower right-hand corner of the DCT matrix. The errors in high frequency coefficients are less sensitive to Human Visual System (HVS) as compared to lower frequency coefficients. Due to this, the higher frequency components can be more easily quantized.

Moreover, DCT soft core is the unit which can be used to perform the Discrete Cosine Transform (DCT). It performs two-dimensional 8 point DCT for the period of 64 clock cycles in pipelined mode. Generally, the two-dimensional DCT transforms an NXN data array into an NXN resultant array. The 2D DCT of a sequence f(x), $0 \leq u \leq N-1$ is defined as

$$c(u,v) = \alpha(u)\,\alpha(v) \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x,y)\cos\left[\frac{\pi(2x}{2}\right.$$

Where C(u,v) denotes the coefficient of the DCT matrix at point (u,v), f(x,y) denotes the spatial domain value at a coordinate (x,y) of the JPEG image array, N denotes the width and height of the image, and a(u), a(v) are known as normalization constants.

After the evaluation of DCT, the data can be reduced to focus the important information into a few DCT results, leaving the remaining some coefficients equal to zero. Resulting the image energy is concentrated in a few DCT coefficients[10].

II. LITERATURE SURVEY

K. Wahid,[1] in year 2011, The architecture is totally based on low complexity Arai Algorithm, which leads to low power realization. These realization is also based on application having FRS section at output stage[1].

R. J. Cintra and F. M. Bayer[2] in year 2011, The Paper focuses on global multiplication which is not problematic. At subsequent signal processing stages it can be embedded after DCT operation[2].

S.Bouguezel, M. O. Ahmad, and M. N. S. Swamy[3] in year 2008, They focuses on the low complexity 8*8 transform for compression, to reduce the size of sent data for which necessary bandwidth is required for digital signal representation[3].

A. Madanayake, R. J. Cintra, D. Onen, V. S. Dimitrov, and L. T. Bruton[5] in year 2011, To completely avoid arithmetic errors within algorithm they employ bivariate AI encoding for maintaining computation[5].

T. Suzuki and M. Ikehara[6] in year 2010, This paper is based on direct lifting of DCT for lossless-to-lossy image coding. The 2-D DCT is evaluated by successive calls of the 1-D DCT which is applied to the column of 8*8 image block then to the rows of transposed which results intermediate calculation[6].

P. K. Meher[7] in year 2006, They focuses on highly concurrent reduced-complexity 2-D systolic array for discrete fourier transform and discrete cosine transform[7].

A. M. Shams, A. Chidanandan, W. Pan, and M. A. Bayoumi[8], in year 2006, Generally focuses on low power high performance DCT architecture, Depending on the interested video signal statistics, at a particular 2-D DCT coefficient quantization noise can have a significant correlation with noise[8].

M. A. Robertson and R. L. Stevenson[9] in year 2005, This paper is based on DCT quantization noise in image compression. In Practical DCT implementation, combating noise injection, noise coupling, and noise amplification is a major concern.

O. Gustafsson, A. G. Dempster, K. Johansson, M. D. Macleod, and L. Wanhammer[10], In this paper simplified design of constant coefficient multiplier are discussed, the method Dempstor and Macleod is required for hardware implementation.

W. Chen, C. Smith, S. Fralick[11], in year 1977 , This paper discusses the fast computational algorithm for Discrete cosine transform. The 2-D DCT calculation has a high degree of computational complexity, So according to the application needs complexity can be minimized.

III. RELATED WORK DCT AND ALGEBRAIC INTEGER ENCODING

Our purpose in employing AI encoding is to allow the arithmetic manipulation of such real numbers in an error-free framework[5]. Originally AI encoding is proposed for digital signal processing. It led to area efficient VLSI video processing with low power consumption [1]. The error-free encoding of the 8-point 1-D DCT elements by means of the AI approach is available. It is observed that the set possesses a high degree of symmetry and that not all elements are required to be explicitly computed (e.g., $\cos(n\pi/16) = -\cos(15\pi/16)$. Moreover, depending on the DCT algorithm employed, only a subset of these elements is in fact required. Considering the DCT fast algorithm by Arai that the required elements for 1-D DCT operation are only[6]:

$m1 = \cos(4\pi/16)$, $m2 = \cos(6\pi/16)$, $m3 = \cos(2\pi/16) - \cos(6\pi/16)$, and $m4 = \cos(2\pi/16) + \cos(6\pi/16)$.

Comparing to Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT) has some advantages:

- High image energy compaction.
- Lower blocking artifacts.
- Real data, coefficients and arithmetic only.
- Effective DCT algorithm.

IV. PROPOSED SCHEME

The architecture is based on the low-complexity Arai algorithm, which formed the building-block of each1-D DCT using AI number representation[3][7].

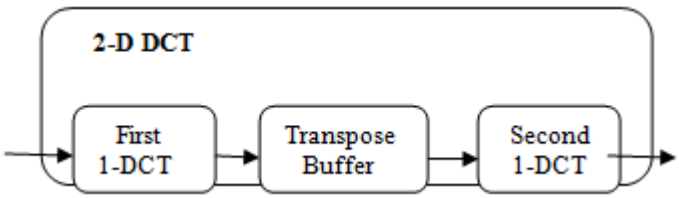

Figure 1- The generic 2-D DCT architecture

The Arai algorithm is a widely used algorithm for video and image-processing applications because of its specialty that is relatively low computational complexity [8]. It is to be noted that the eight-point Arai algorithm only needs five multiplications to generate the eight output coefficients. The algorithm chosen calculates the DCT in one dimension (1-D DCT) and the 2-D DCT calculation is made using its separate property. Thus, using two 1-D DCT we can successfully generate the 2-D DCT coefficients.

In an 8x8 input matrix, the first 1-D DCT will perform row-wise and the second 1-D DCT will perform column-wise on the outputs of the first 1-D DCT. This simple decomposition will reduce the complexity of the calculation [4].

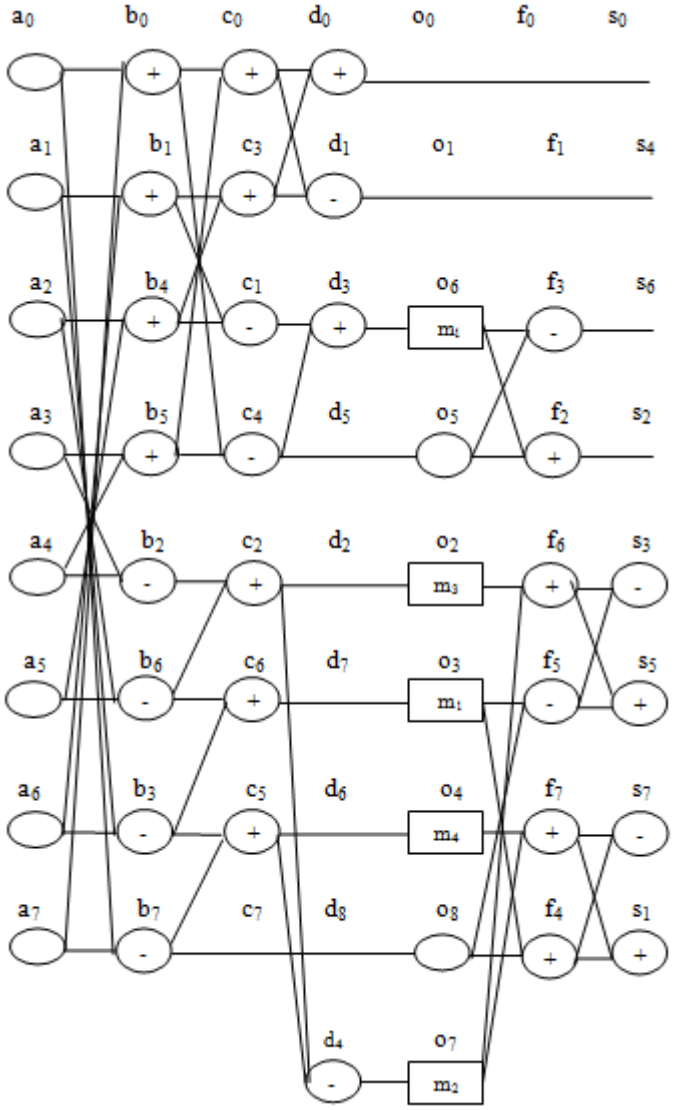

Figure 2- Signal Flow Graph of Arai

V. IMPLEMENTATION

The 2-D DCT inputs in our design are matrixes of 8x8 elements eight-bit wide each. The first 1-D DCT receives the bit and further processes these matrixes in a row-wise order. The transpose buffer receives the row-wise bits and sends the column-wise inputs to the second 1-D DCT architecture. The second architecture will processes the column-wise data and gives the output in a column- wise manner.

The complete algorithm is performed in following steps:

Step1:

b0:=a0 + a7; b1:=a1+a6; b2:=a3- a4; b3:=a1- a6;

b4:=a2+ a5; b5:=a3 +a4; b6:=a2- a5; b7:=a0- a7;

Step2:

c0:=b0 + b5; c1:=b1 - b4; c2:=b2 + b6; c3:=b1+b4;

c4:=b0 - b5; c5:=b3 +b7; c6:=b3 + b6; c7:=b7;

Step 3:

d0:=c0 + c3; d1:=c0 - c3; d2:=c2; d3:=c1+c4; d7:=c6;

d4:=c2 - c5; d5:=c4; d6:=c5; d8:=c7;

Step 4:

e0:=d0; e1:=d1; e2:=m3*d2; e3: =m1*d7; e7: =m2*d4;

e4:=m4*d6;e5:=d5; e6:=m1*d3; e8 : =d8;

Step 5:

f0:=e0; f1:=e1; f2:=e5+e6; f3:=e5 - e6;

f4:=e3 +e8; f5:=e8 - e3; f6:=e2+e7; f7:=e4+e7;

Step 6:

s(0):=f0; s(1):=f4+ f7; s(2):=f2; s(3):= f5 -f6;

s(4):=f1; s(5):=f5+f6; s(6):=f3; s(7):= f4 - f7;

Where {a_i} are input elements, {Si} are scaled DCT coefficient

m1 = cos (π/4.0);

m2 = cos (π*3/8);

m3 = cos (π/8) - cos (π*3/8);

m4 = cos (π*/8) +cos (π*3/8);

Table I Ai Encoding of Arai DCT Coefficients

	a0	a1	a2	a3
m1	-2	0	1	0
m2	0	-3	0	1
m3	0	4	0	-1
m4	0	-2	0	1

Table II 2-D Ai Encoding of Arai DCT Coefficients

m1	m2	m3	m4
$\begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix}$	$\begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}$	$\begin{pmatrix} 0 & 0 \\ 2 & 0 \end{pmatrix}$	$\begin{pmatrix} 0 & 2 \\ 0 & 0 \end{pmatrix}$

As shown in above figure1. There are two 1-D DCT blocks, each uses eight clock cycles and its latency is 48 clock cycles. When the pipeline is full the complete 8*8 matrix processed at 64 clock cycles each. The transpose

buffer latency is 64 clock cycles and to generate new transpose matrix 64 clock cycles are required. The number of bits of two 1-D DCT architecture will be different for each pipeline stage.

Table III Bit Width Differences

Pipeline stage	First 1-D DCT width	Second 1-D DCT width
1	9	13
2	10	14
3	11	15
4	11	15
5	12	15
6	12	15

The 8x8 block of DCT coefficients is ready for compression by quantization process. After DCT evaluation, the image obtained is described in terms of its frequency domain in detail. However, the human eye cannot predict changes that it has very bright or very dim colors. JPEGs can be compressed further by rounding the observed changes in frequency which cannot be distinguish by the human eye[9].

Each number in the 8*8 block is divided by the corresponding number at the coordinates of the quantization matrix and get rounded to an integer with respect to JPEG image.

Huffman coding is nothing but an entropy encoding algorithm we generally use for lossless data compression applications. The basic idea behind Huffman coding is to assign the symbol to the particular compressed slot of data with minimum redundancy.All operation performs on Scaled output mode. In Scaled Output Mode, the repeated and unused coefficient is removing from output coefficient matrix of DCT.

The Arai Algorithm which is used for the calculation also uses FIFO as a storage element. It is the First in First out process.

A data structure that holds elements in the order they are received and provides access to those elements using the policy. Generally there are three types of FIFO:

a. Shift registers FIFO.
b. Exclusive read/write FIFO.
c. Concurrent read/write FIFO.

Our main aim is to achieve more accuracy, low power, low area by designing and analysis of AI encoding for Arai fast Algorithm to minimize the amount of DCT calculations.

So after the analysis on a Xilinx Virtex-7 XC7V285T FPGA device we get the report on device utilization in terms of area.

TABLE IV

Report on Utilization of Devices			
Utilization of Logic	**Device Used**	**Available Device**	**Total Utilization**
Slice registers	**544**	**357600**	**0%**
Slice LUTs	**869**	**178800**	**0%**
Fully used LUT-FF Pairs	**398**	**1015**	**39%**
IOBs	**25**	**600**	**4%**
BUFG/BUFG CTRLs	**1**	**32**	**3%**
DSP48E1s	**4**	**700**	**0%**

V. CONCLUSION

The work presented here focuses on implementation of improved 8*8 2-D DCT architecture using Arai fast algorithm to minimize DCT calculation. Arai employed with its low computational complexity, hence popularly used. It is compatible with various FPGA devices such as Xilinx Virtex[11].

Here the algorithm is operational at a clock frequency of 415.239 MHz on a Xilinx Virtex-7 XC7V285T FPGA device with total delay of 1.791ns. Of which the logical delay is 1.512ns and routing delay is 0.279ns. Hence the speed of the DCT architecture gets increased.

Our architecture is now fast and more improved architecture as compared to previous designed DCT 8*8 architecture. The design allowed each 64 coefficients to be computed at different precision levels, so that each choice of precision will affect that particular coefficient. Due to this their will be full control over the 2-D DCT computation to any degree of precision as per designer requirement [12][13].

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