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DESIGN OF 8 PORT ROUTER FOR NOC USING VERILOG

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ABSTRACT

Multiprocessor system on chip is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. Researchers pursued a scalable solution to this problem i.e. Network on Chip (NOC). Network on chip architecture better supports the integration of SOC consists of on chip packet switched network. The proposed design of 8 port router is simulated and synthesized in Xilinx ISE 9.2i and the source code is written in Verilog.

Keywords: Network on Chip, 8 port router, Xilinx ISE 9.2i.

I. INTRODUCTION

as per Moore's law the density of chip doubles every 18 months, so the parameters of a single chip get affected due to increase of processing elements on a chip. NOC is a packet switched on-chip data transfer network that solves challenges faced by SOC of bus based communication. The basic ingredients of NOC are topology which defines the communication architecture, routing technique which decides how the data is routed from sender to receiver, routers and switching technique which determines when the data flow through the routers.

NOC used only point to point wires for all network sizes and it increases the utilization of wires. The focus of paper is design of Network on chip five port routers. The effective on chip communication is achieved by router's routing functionality and efficient arbitration [1]. The main goal of this paper is the design of power and area efficient on chip router.

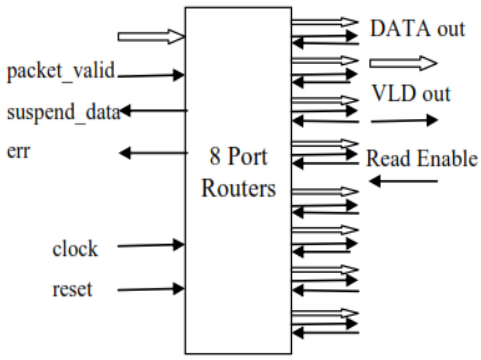
II. OVERVIEW

A variety of interconnection schemes are currently in use, including crossbar, buses and NOCs. Of these, later two are dominant in research community. However buses suffers from poor scalability because as the number of processing elements increases, performance degrades dramatically. Hence they are not considered where processing elements are more. To overcome this limitation attention has shifted to packet-based on-chip communication networks, known as Network-On-Chip (NOC).

III.ROUTER

System on chip is a complex interconnection of various functional elements. It creates communication bottleneck in the gigabit communication due to its bus based architecture. Thus there was need of system that

explicit modularity and parallelism, network on chip possess many such attractive properties and solve the problem of communication bottleneck. It basically works on the idea of interconnection of cores using on chip network. The communication on network on chip is carried out by means of router, so for implementing better NOC, the router should be efficiently design.



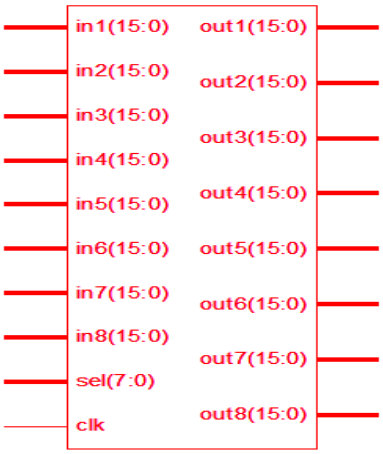


Figure-1: Block diagram of 8 port router Figure-2: Synthesized 8 port block diagram in Xilinx ISE

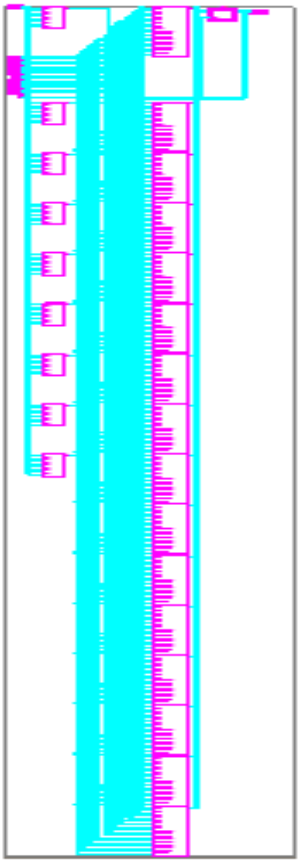


Figure-3: Schematic of 8 Port router

IV. RESULT ANALYSIS

Design Statistics

IOs : 265

Cell Usage :

BELS : 125

GND : 1

LUT2 : 18

LUT3 : 4

LUT4 : 96

MUXF5 : 5

VCC : 1

FlipFlops/Latches : 16

FDS : 16

Clock Buffers : 1

BUFGP : 1

IO Buffers : 264

IBUF : 136

OBUF : 128

Device utilization summary:

Selected Device : 3s50pq208-5

Number of Slices:	69	out of	768	8%
Number of Slice Flip Flops:	16	out of	1536	1%
Number of 4 input LUTs:	118	out of	1536	7%
Number of IOs:	265			
Number of bonded IOBs:	265	out of	124	213%
Number of GCLKs:	1	out of	8	12%

Timing Summary:

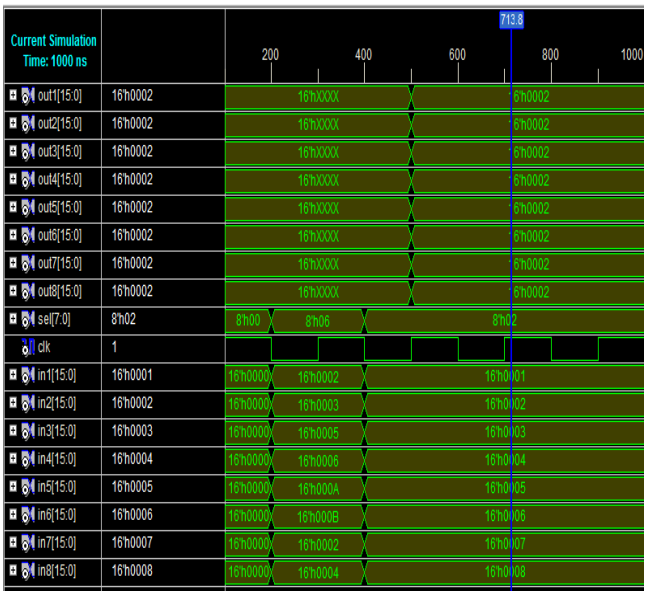
Minimum period: 2.259ns

Minimum input arrival time before clock: 9.966ns

Maximum output required time after clock: 6.490ns

Maximum combinational path delay: No path found

V. SIMULATION RESULTS



VI. CONCLUSION

The proposed design of 8 port router is simulated and synthesized in Xilinx ISE 9.2i and the source code is written in Verilog. This proposed design has high speed and less delay. The Total delay is 2.259ns.

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