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OPTIMIZING MULTIPLIER DESIGN USING VEDIC MATHEMATICS

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ABSTRACT

An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). Application of the Sutras saves a lot of time and effort in solving the problems, compared to the formal methods presently in vogue.

A Simple ALU which perform multiplication and division has been presented. Multiplier is designed using Urdhva Tiryakbhyam(Vertical and cross wise) sutra where addition of partial product is carried out using kogge stone adder. In this paper the comparison of vedic mathematics and conventional mathematical method is carried out to know the best architecture for ALU design w,r,t power and delay characteristics. The design of architecture are done in Verilog language and the tool used for simulation is Xilinx 9.1 ISE

Keywords: Central Processing Unit, Graphics Processing Units, Urdhva Tiryakbhyam, , Verilog.

I. INTRODUCTION

Multipliers and Dividers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer high speed, low power consumption, regularity of layout and hence less area or even combination of them in one module thus making them suitable for various high speed, low power and compact VLSI implementation.

Survey shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operations dominate the execution time. Vedic mathematics is a unique technique of carrying out mathematical computations and it has its roots in the ancient Indian Mathematics. Vedic Mathematics is used in many ways in solving problems. This system helps to reducing finger counting and also helps in remembering too many questions. Vedic mathematics helps us reduce common small mistakes as this method is direct, simple and best part is that it keeps the minds alert.

Our brain is like a muscle, just like other parts of our body and it requires regular exercise. When we practice Vedic Mathematics, we make use of both left and right brain. Left brain is responsible for the language and processes in a logical and sequential order while the right brain or say right hemisphere is more visual and processes intuitively, holistically, and randomly which boosts memory and concentration. As we are doing calculations mentally without using pen and paper, we are actually increasing our concentrating abilities.

Vedic Mathematics is the world's fastest calculating system in terms of shortcuts. It is 10 to 15 times faster than conventional system of learning. Vedic Mathematics is a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved .There are set of defined formulas which

one needs to memorize and understand. Shree Bharti Krishnajee Maharaj rediscovered these methods from vedas between 1911 to 1918 which is based on 16 sutras.

II. VEDIC SUTRAS

Vedic Math essentially rests on the 16 Sutras or mathematical formulas as referred to in the Vedas. The sixteen sutras and their corollaries are as follows [3]:

- Shunyamanyat – If one is in ratio, the other is zero
- Chalana-Kalanabyham – Differences and Similarities.
- Ekadhikina Purvena – By one more than the previous one
- Ekanyunena Purvena – By one less than the previous one
- Gunakasamuchyah – The factors of the sum is equal to the sum of the factors
- Gunitasamuchyah – The product of the sum is equal to the sum of the product
- Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10
- Paraavartya Yojayet – Transpose and adjust.
- Puranapuranabyham – By the completion or noncompletion
- 10.Sankalana-vyavakalanabhyam – By addition and by subtraction
- Shesanyankena Charamena – The remainders by the last digit
- Shunyam Saamyasamuccaye – When the sum is the same that sum is zero
- Sopaantyadvayamantyam – The ultimate and twice the penultimate
- Urdhva-tiryakbyham – Vertically and crosswise
- Vyashtisamanstih – Part and Whole
- Yaavadunam – Whatever the extent of its deficiency

III. PROPOSED ARCHITECTURE

3.1 “Uradhya Tiryakbhyam”Sutra

The meaning of this sutra is "Vertically and crosswise" and it is applicable to all the multiplication operations. Fig. 1 represents the general multiplication procedure of the 4x4 multiplication. This procedure is simply known as array multiplication technique[1,2].

Line diagram for multiplication of 456 and 789 is shown in Fig 2.Digits in two ends of line are multiplied and then the result is added with the precious carry. when we find more lines in one step, all results are added to previous carry. Interestingly, the least significant digit of the number thus obtained acts as in of the result digits and thus the rest act as the carry for the next step. Note that initial carry is zero.

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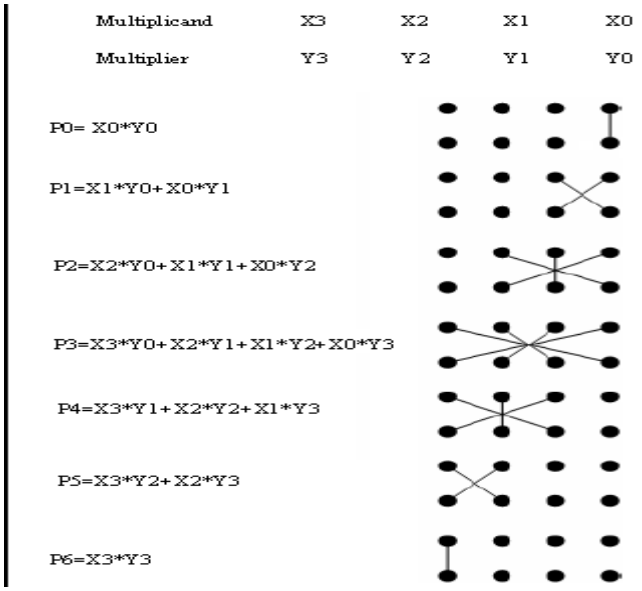

Fig 1: Multiplication procedure using "Urdhva-tiryakbyham " sutra

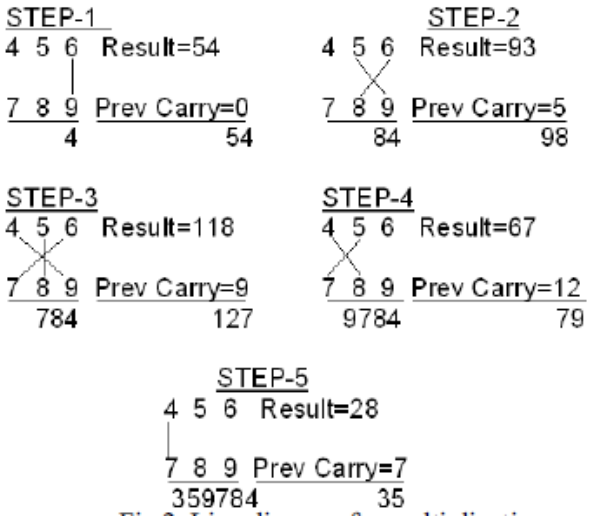

Fig 2:Line diagram for multiplication

3.2 Kogge stone adder

The Kogge–Stone adder is a parallel prefix form carry look-ahead adderThis adder structure has minimum logic depth, and full binary tree with minimum fun-out, resulting in a fast adder but with a large area.

An example of a 4-bit Kogge Stone adder is shown in Fig.3 to the right. Each vertical stage produces a "propagate" and a "generate" bit, as shown. The culminating generate bits (the carries) are produced in the last stage (vertically), and these bits are XOR'd with the initial propagate after the input (the red boxes) to produce the sum bits. E.g., the first (least-significant) sum bit is calculated by XORing the propagate in the farthest-right red box (a "1") with the carry-in (a "0"), producing a "1". The second bit is calculated by XORing the propagate in second box from the right (a "0") with C0 (a "0"), producing a "0".

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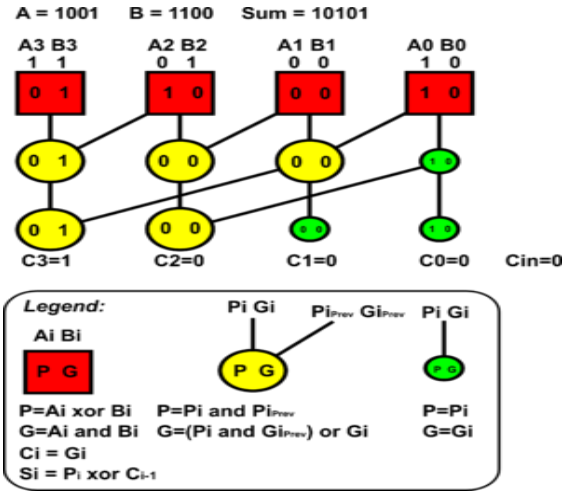

Fig 3: Example of a 4-bit Kogge–Stone adder with 0 carry-in.

Expansion of 4 bit Kogge stone adder is as shown below

S0 = (A0 XOR B0) XOR Cin

S1 = (A1 XOR B1) XOR ((A0 AND B0)or(A0 XOR B0) AND Cin)

S2 = (A2 XOR B2) XOR (((A1 XOR B1) AND ((A0 AND B0)or(A0 XOR B0) AND Cin)) OR (A1 AND B1))

S3 = (A3 XOR B3) XOR ((((A2 XOR B2) AND (A1 XOR B1)) AND ((A0 AND B0)or(A0 XOR B0) AND Cin)) OR (((A2 XOR B2) AND (A1 AND B1)) OR (A2 AND B2)))

S4 =(A3 AND B3) OR (A3 XOR B3) AND ((((A2 XOR B2) AND (A1 XOR B1)) AND ((A0 AND B0)or(A0 XOR B0) AND Cin)) OR (((A2 XOR B2) AND (A1 AND B1)) OR (A2 AND B2)))

3.3 Wallace tree multiplier

A Wallace tree is a conventional multiplier and is an efficient hardware implementation of a digital circuit that multiplies two integers. Algorithm for 4 bit Wallace tree multiplier is as shown in Fig 4

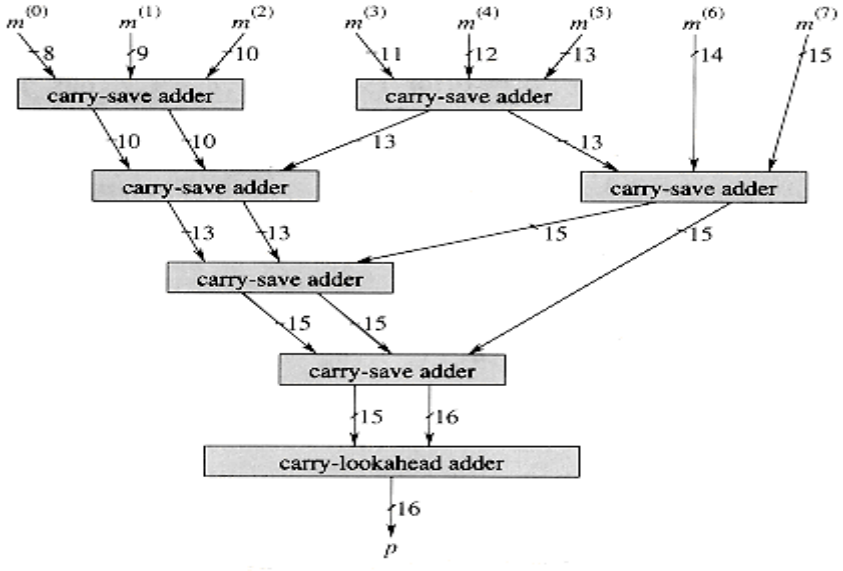

Fig 4: Algorithm for 4 bit Wallace tree multiplier

IV. IMPLEMENTATION

Multiplication algorithm is implemented in Verilog HDL and logic simulation is done in Modelsim Simulator; the synthesis and FPGA implementation is done. The design is optimized for speed and area using Xilinx, Device Family: spartan3.

IV. RESULT

The 4*4 bit multiplier is designed in verilog HDL using Xilinx and simulated using Modelsim Simulator.

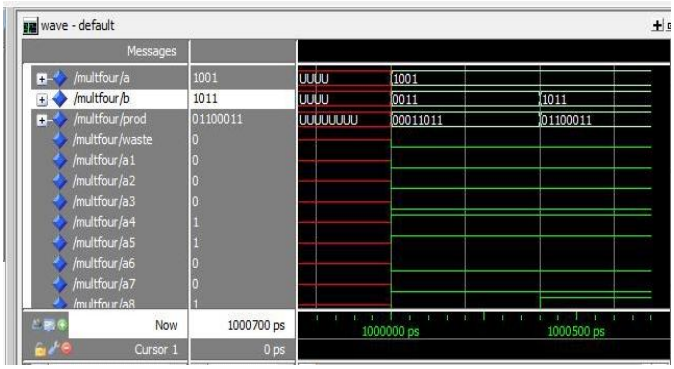

Fig 5: Simulation result of vedic multiplier with kogge stone adder

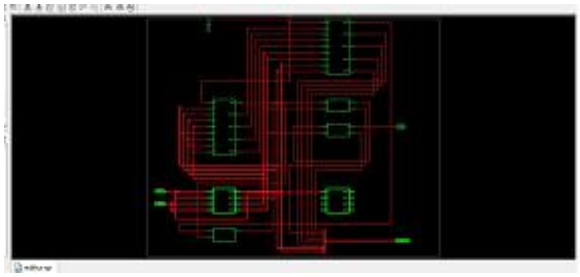

Fig 6:RTL schematic of vedic multiplier with kogge stone adder

V. COMPARISON

The comparision of vedic multiplier and Wallace tree multiplier wrt delay is as shown in table

Type	Bits	Delay(ns)
Vedic multiplier with kogge stone adder	4	5.12
Wallace tree multiplier	4	7.168

Table 1: Comparison of vedic and Wallace tree multiplier

VI. CONCLUSION

In this paper the comparison of vedic multiplication and conventional multiplication method is carried out to know the best architecture for ALU design w,r,t power and delay characteristics. vedic multiplication is proved to be the best architecture for ALU design.

REFERENCES

[1] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho, "Multiplier design based on ancient Indian Vedic Mathematics," 2008 International SoC Design, pp 65-68.

[2] Gensuke Goto,"High Speed Digital Parallel Multiplier", United State ,Patent-5,465,226, November 7 1995.

[3] "Vedic Mathematics- Methods", Sri Sathya Sai Veda Pratishtan.