International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 12, December 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

DESIGN OF HIGH RESOLUTION DPWM USING GENERAL-PURPOSE FPGA

Prof. Munmun Das[1], Ms. Kokate Pratibha[2],
Ms. Lasure Pooja[3] , Mr. Khatake Dattatraya[4]

[1,2,3,4] *Dept. of Electronics & Tele-communication Eng.*
PGMCOE, Wagholi, Pune, Maharashtra, (India)

ABSTRACT

The pulse width modulation (PWM) principle is widely used in power electronics applications for controlling power converters. This article deals with the generation PWM signals with variable duty from 0% to 100% using VHDL and its application in field programmable gate arrays. Nowadays recent developments in semiconductor technology enable the use of high switching frequencies. So the design of power converters requires a high resolution high frequency pulse width modulators (HRPWMs) in order to reduce the size and cost, and improved dynamic behavior and power density.

Keywords: PWM(Pulse Width Modulation)

I INTRODUCTION

Pulse width modulation (PWM) is a powerful technique for controlling analog circuits with a processor's digital outputs. Engineers use microcontrollers largely to build control system, but the microcontrollers are going to disappear with the appearance FPGA. Because with FPGA, all control system features can be added to a single chip, and new functions can be used. FPGA implementation of PWM is selected because FPGA can process information faster, controller architecture can be optimized for space or speed[1].

A PWM signal is not constant, the main parameter is a duty cycle *D* that is a part of PWM period and describes the proportion of on time to regular interval[2]. The equation describes the duty cycle as the following:

$$D=\tau/T$$

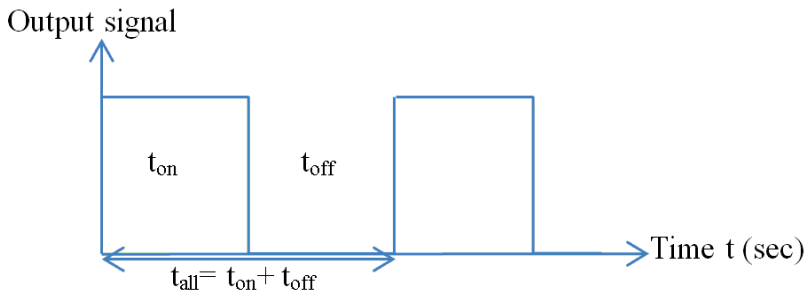
Where: $0 \leq D \leq 1$

Thus the output signal is calculated in equation:

$$Output=D*input=(Ton/ts)*input$$

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 12, December 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

Figure shows the duty cycle of PWM



II STRATEGY OF BUILDING A PWM SIGNALS IN FPGA USING VHDL

The principle of PWM work is required to design PWM. Figure illustrates the principle of work:

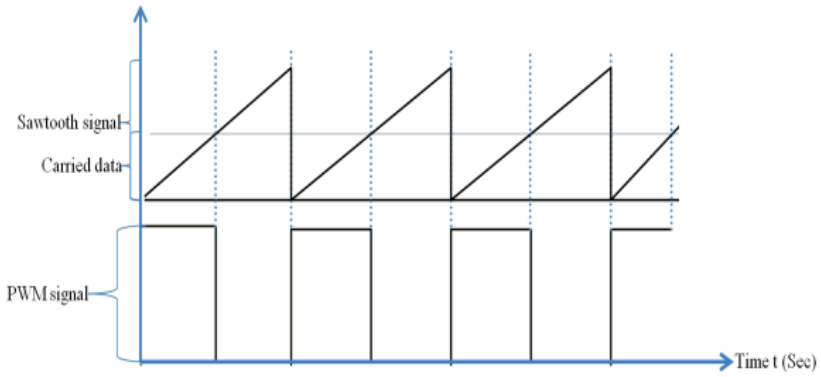


Fig: Principle PWM

As figure shown the design of processor that generates the signals, which give the output of PWM, requires a comparator that compares between two values[3]. The first value represents the sawtooth signal and the second value represents the data that is entered by using switches or buttons on the FPGA board[4]. The input signal can take another form such as sinusoidal signal. When the design requires generating a sinusoidal PWM in FPGA, it must generate LUT using MATLAB and these data must be saved in block memory to control the PWM output[5].

III THE PROPOSED PWM ARCHITECTURE

The register stores the input to be processed .So when load signal is '1' the register provides input to output. The counter used is 8 bit up-counter. The N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit counter, by means of a comparator.

When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period.

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 12, December 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

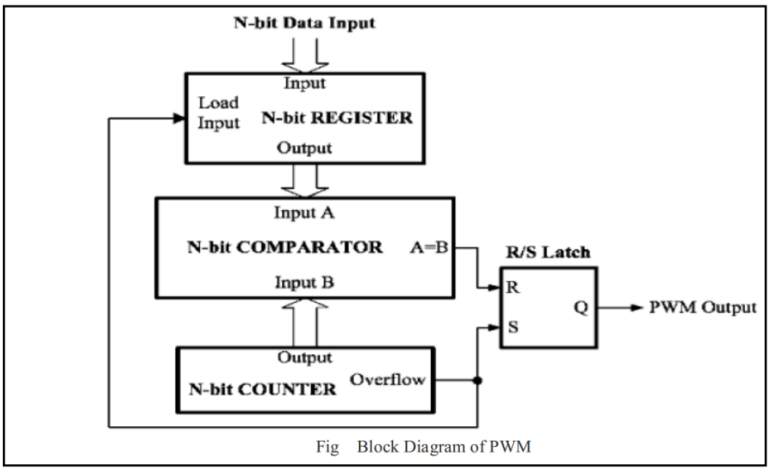


Fig Block Diagram of PWM

Also, the counter overflow signal is used to load the N-bit data input to the input register. R S latch is used to set or reset the output. When ‘r’ signal is ‘1’ output is reset to ‘0’.When ‘s’ signal is ‘1’ output is set to ‘1’.

The duty cycle is given from the following equation:

Duty Cycle = Data Value/2n

where, Data Value is the N-bit input data value.

IV CONCLUSION

The generation of PWM signals is discussed using VHDL based on FPGA. A board SPARTAN3A is used as a hardware and ISE14.4 XILINX is used as software. A PWM counter and the algorithm are designed that allow to enter the data using two push buttons on the board. The comparator is necessary to compare between the data that generate PWM signals. The generated PWM signals have a fixed frequency (11.8 KHz) depended on the frequency of sawtooth, and a variable duty cycle that changes from 0% to 100%. But the frequency can be changed using DCM manager, without editing the program. The PWM developed can be used in many diverse and complex applications like robotics, motor and motion control.

Literature Cited

- In the past, when only partial power was needed, a rheostat is used to adjust the amount of current flowing through the motor, but also wasted power as heat in the resistor element.
- Whereas, in FPGA implementation of PWM, FPGA can process information faster and it is powerful technique for controlling analog circuits.

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

REFERENCES

[1]Navarro, O. Luc´ıa, L. Barrag´an, J. Artigas, I. Urriza, and O. Jim´enez,"Synchronous FPGA -based high-resolution implementations of digital pulse-width modulators," IEEE Trans. Power Electron. , vol. 27, no. 5, pp. 2515

–2525, May 2012.

[2] G. Feng, E. Meyer, a nd Y. F. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC -to- DC converters," IEEE Trans. Power Electron. , vol. 22, no. 4, pp. 1489– 1498, Jul. 2007.

[3] S. Huerta, Angel De Castro, O. Garcia, J.A. Cobos, "FPFA -based digital pulsewidth modulator with time resolution under 2 ns ." IEEE Trans. Power Electron., vol 23 , no. 6, pp. 3135-3141, Nov. 2008.

[4] Survey of digital control for power converters.

[5] Mor Mordechai Peretz, and Shmuel (Sam) Ben-Yaakov "Digital Control of Resonant Conver ters: Resolution Effects on Limit Cycles" IEEE Trans. Power Electon ., Vol. 25, no. 6,pp. 1652-1660, June 2010