A High Step-Down Transformerless Single-Stage Single-Switch AC/DC Converter

B. Rajesh
Assistant Professor EEE Department Dhruva Institute of Engineering and Technology (India)

ABSTRACT

This paper presents a high step-down transformerless single-stage single-switch ac/dc converter suitable for universal line applications (90–270 V RMS). The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.

Index Terms—Direct power transfer (DPT), integrated buck–buck–boost converter (IBuBuBo), power-factor correction (PFC), single-stage (SS), transformerless.

I. INTRODUCTION

INGLE-STAGE (SS) ac/dc converters have received much attention in the past decades because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]–[7]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g., ≤48V), this high intermediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement [11]. Also, in some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries, and subway applications [12]), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other
drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14]. To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters [9], [10], [15]–[18] employ different PFC cells to reduce the intermediate bus voltage. Among those converters, [9] and [15] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In [10], [17], and [18], the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [18] and [10] process power at least twice resulting in low power efficiency. Moreover, the reported converters, in [16], and [17], consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the converter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in the Section V.

In this paper, an integrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved.
Fig. 1. (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms.

Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve:
1) low intermediate bus and output voltages in the absence of transformer;
2) simple control structure with a single-switch;
3) positive output voltage;
4) high conversion efficiency due to part of input power is processed once and
5) input surge current protection because of series connection of input source and switch.

The paper is organized as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and followed by design consideration with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V, respectively. Finally, conclusion is stated in Section VI.

II. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L₁, S₁, D₁, C₀, and Cᴮ) and a buck–boost dc/dc cell (L₂, S₁, D₂, D₃, C₀, and Cᴮ) is illustrated in Fig. 1(a). Although L₂ is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L₂ is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L₁ and L₂ at the beginning of each switching cycle t₀. Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A (vᵢᵣ(θ) ≤ Vᴮ + Vₒ): When the input voltage vᵢᵣ(θ) is smaller than the sum of intermediate bus voltage Vᴮ and output voltage Vₒ, the buck PFC cell becomes inactive and does not shape the line current around...
zero-crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f). Fig. 3(a) shows its key current waveforms.

1) Stage 1 (period $d_1 T_s$ in Fig. 3) [see Fig. 2(a)]: When switch $S_1$ is turned ON, inductor $L_2$ is charged linearly by the bus voltage $V_B$ while diode $D_2$ is conducting. Output capacitor $C_o$ delivers power to the load.

2) Stage 2 (period $d_2 T_s$ in Fig. 3) [see Fig. 2(b)]: When switch $S_1$ is switched OFF, diode $D_3$ becomes forward biased and energy stored in $L_2$ is released to $C_o$ and the load.

3) Stage 3 (period $d_3 T_s - d_4 T_s$ in Fig. 3) [see Fig. 2(f)]: The inductor current $i_{L_2}$ is totally discharged and only $C_o$ sustains the load current.

Mode B ($v_{in}(\theta) > V_B + V_o$): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

1) Stage 1 (period $d_1 T_s$ in Fig. 3) [see Fig. 2(c)]: When switch $S_1$ is turned ON, both inductors $L_1$ and $L_2$ are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($v_{in}(\theta) - V_B - V_o$), while diode $D_2$ is conducting.

2) Stage 2 (period $d_2 T_s$ in Fig. 3) [see Fig. 2(d)]: When switch $S_1$ is switched OFF, inductor current $i_{L_1}$ decreases linearly to charge $C_B$ and $C_o$ through diode $D_1$ as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in $L_2$ is released to $C_o$ and the current is supplied to the load through diode $D_3$. This stage ends once inductor $L_2$ is fully discharged.

3) Stage 3 (period $d_3 T_s$ in Fig. 3) [see Fig. 2(e)]: Inductor $L_1$ continues to deliver current to $C_o$ and the load until its current reaches zero.

4) Stage 4 (period $d_4 T_s$ in Fig. 3) [see Fig. 2(f)]: Only $C_o$ delivers all the output power.

III. DESIGN CONSIDERATIONS

To simplify the circuit analysis, some assumptions are made as follows:

1) all components are ideal;
2) line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{p.k} \sin(\theta)$ where $V_{p.k}$ and $\theta$ are denoted as its peak voltage and phase angle, respectively;
3) both capacitors $C_B$ and $C_o$ are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;
4) the switching frequency $f_s$ is much higher than the line frequency such that the rectified line input voltage $|v_{in}(\theta)|$ is constant within a switching period.
A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time \( \alpha \) and \( \beta \) can be expressed as

\[
\alpha = \arcsin \left( \frac{V_T}{V_{p_k}} \right) \quad \beta = \pi - \alpha = \pi - \arcsin \left( \frac{V_T}{V_{p_k}} \right)
\]

where \( V_T \) is the sum of \( V_B \) and \( V_o \). Thus, the conduction angle of the converter is

\[
y = \beta - \alpha = \pi - 2\arcsin \left( \frac{V_{p_k}}{V_T} \right)
\]

From the key waveforms (see Fig. 3), the peak currents of the two inductors are

\[
i_{L_{p_k}} = \frac{v}{L_1} \left[ d_1 T_s \quad \alpha < \theta < \beta \right. \]

\[
i_{L_{p_k}} = 0, \quad \text{otherwise}
\]
where \( T_s (1/f_s) \) is a switching period of the converter. In (3) and (4), the dependency of \( i_{L1 pk} \) on \( \theta \) has been omitted for clarity. It is noted that \( L_2 \) does not contribute in (3) even though it is on the current return path of the PFC cell.

**Fig. 3. Key waveforms of the proposed circuit**

In addition, by considering volt–second balance of the \( L_1 \) and \( L_2 \), respectively, the important duty ratio relationships can be expressed as follows:

\[
d_2 + d_3 = \begin{cases} 0, & 0 < \theta < \beta \\ \frac{v_m(\theta) - V_T}{V_B} \frac{d_1}{d_1}, & \alpha < \theta < \beta \\ \end{cases}
\]

By applying charge balance of \( C_B \) over a half-line period, the bus voltage \( V_B \) can be determined. From Fig. 3, the average current of \( C_B \) over a switching and half-line periods are expressed as:

\[
< i_{C_B} >_{SW} = \frac{1}{2} \left( i_{L1 pk} (d_1 + d_2 + d_3) - L_2 \frac{V_B}{R_L} \right)
\]

\[
\frac{\delta_1}{2} \left( |V_{in}(\theta)| - |V_T| \right) \frac{|V_B|}{L_1} \tau_t \frac{d_1}{L_2} (7)
\]

and

\[
< i_{C_B} >_{SW} = \frac{1}{2 \pi} \frac{\pi}{V_{pk} V_T (2 + \frac{A}{2}) - B} \left( \frac{\pi V_B}{2} \right)
\]

where the constants \( A \) and \( B \) are
Putting (8) to zero due to the steady-state operation, this leads to

\[
V_B = \frac{M V_{p}^2}{\sqrt{2}} \times \frac{2\pi \arcsin \left( \frac{V_B + V_o}{V} \right)}{2(\sqrt{V_B^2 + V_o^2})(V_{p1}^2 + V_B^2 + V_o^2)(V_{p1} - V_B - V_o)}
\]

where \(M\) is the inductance ratio \(L_2 / L_1\).

As observed from (11), the bus voltage \(V_B\) can be obtained easily by numerical method. It is noted that \(V_B\) is independent on the load, but dependent on the inductance ratio \(M\). Fig. 4 depicts the relationship among \(V_B\), rms value of the line voltage, and inductance ratio \(M\). It is noted that the bus voltage is kept below 150 V at high-line input condition.

Similarly, the instantaneous and average input currents of the proposed circuit are

\[
\langle i_{\text{in}} \rangle = \frac{\int_{0}^{\pi / \omega} (V_{\text{in}}(\theta) - V_T \sin^2 \theta) d\theta}{\int_{0}^{\pi / \omega} 1 d\theta} = \begin{cases} \frac{V_{\text{in}}(\theta) - V_T \sin^2 \theta}{2L_1} & 0 < \theta < \beta \\ \frac{1}{2L_1} & \text{otherwise} \end{cases}, \quad \alpha < \theta < \beta
\]

and
Using (12) and (13), the rms value of the input current, average input power and power factor are given by

\[
I_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (i_{\text{in}} > s_{\text{w}}) d\theta} = \frac{1}{2\pi L} \left[ V_{pk} E - yV_T \right]. \quad (13)
\]

Using (12) and (13), the rms value of the input current, average input power and power factor are given by

\[
P_{\text{in}} = \frac{\pi}{2} \frac{\beta}{\alpha} \left( \frac{I_{\text{rms}} > s_{\text{w}}}{\pi} \right)^2 d\theta = \frac{2}{1} \frac{V}{A} \left( \frac{A}{\pi} \right)^2 \frac{1}{\pi} \left( \frac{2}{2} \right) \frac{V}{A} \left( \frac{A}{\pi} \right)^2 \frac{1}{\pi} \left( \frac{2}{2} \right).
\]

(14)

\[
PF = \frac{P_{\text{in}}}{\frac{1}{2} \pi \left( \frac{V}{A} \right)^2 \left( \frac{A}{\pi} \right)^2} = \frac{2}{1} \frac{V}{A} \left( \frac{A}{\pi} \right)^2 \frac{1}{\pi} \left( \frac{2}{2} \right) \frac{V}{A} \left( \frac{A}{\pi} \right)^2 \frac{1}{\pi} \left( \frac{2}{2} \right).
\]

(15)

Fig. 5 exhibits the variation of power factor as a function of line input voltage and the inductance ratio M of the converter.

B. Condition for DCM

To ensure both cells working in DCM mode throughout the ac line period, we must determine their critical inductance first. To allow \( L_1 \) working in DCM and from (5), we have the following inequalities:

\[
d_2 + d_3 \leq 1 - d_{\text{PFC}} \quad (17)
\]

and

\[
d_{\text{PFC}} \leq \frac{V_T}{\frac{1}{2} \pi \left( \frac{V}{A} \right)^2 \left( \frac{A}{\pi} \right)^2}, \quad \alpha < \theta < \beta \quad \text{otherwise} \quad (18)
\]

where \( d_{\text{PFC}} \) is the maximum \( d_1 \) of the PFC cell. For the buck–boost dc/dc cell working in DCM mode, the following inequality must be held:

\[
d_2 \leq 1 - d_{\text{DC/DC}} \quad (19)
\]

From (6) and (19), the maximum \( d_1 \) of the dc/dc cell is

\[
d \leq \frac{V_0}{V_0 + V_B} = V_T \quad (20)
\]

Due to sharing switch in both cells of the converter, the maximum duty cycle \( d_{\text{max}} \) of the proposed converter is

\[
d_{\text{max}} = \min(d_{\text{PFC}}, d_{\text{DC/DC}}), \quad \alpha < \theta < \beta \quad \text{otherwise} \quad (21)
\]

By applying input–output power balance of the PFC cell and substituting (21) into (15), the critical inductance \( L_{1_{\text{crit}}} \) is given by
where RL min is denoted as the minimum load resistance of the converter.

For the dc/dc cell sustaining all the power to the load under the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance $L_2$ crit can be determined. The input power of the dc/dc cell in Mode A is given by

$$ P_{DC/DC} = \frac{<I_{DC/DC}>}{\pi} \quad 0 < \theta < 2\pi $$

where $<I_{DC/DC}>$ is the instantenous input current of dc/dc cell.

Hence, by substituting (21) into (23), the critical inductance $L_2$-crit is given by

$$ L_{2,crit} = \frac{R_{L,\text{min}}V_B^2T_s}{2V_o^2} \frac{d_1^2}{d_{f,\text{max}}^2} $$

C. Components Stresses

Before embarking on calculating stresses on the devices, there are two characteristics of the circuit to be clarified. Interestingly, the current passing through the diode $D_2$ is the difference of current between $i_L 2$ and $i_L 1$ at the time interval $d_1 T_s$. Both inductor currents flows into the diode at the interval, but in opposite direction. In addition, unlike the boost-type single-stage ac/dc converter, the current of the switch $S_1$ is $i_L 2$, but not the superposition current of both inductors. Thus, the simultaneous currents of the diode $D_2$ and switch $S_1$ at interval $d_1 T_s$ are

$$ i_{D_2} = i_L 2 - i_L 1 $$

$$ i_{S_1} = i_L 2 $$

The rms current stresses on the diodes and switch are deter-mined by averaging their rms current in a switching cycle over a half-line period. The rms current stress on the diode $D_1$ over a switching cycle is

$$ i_{D_1,\text{rms}} = max \left\{ \frac{T_s}{L_1} \left[ \frac{d_1}{3} \left( \frac{\alpha}{\beta} - \frac{T_s}{\beta} \right) \right] \right\} \left( \frac{\sqrt{V_o^2}}{3V_T} \right) $$

$$ i_{S_1,\text{rms}} = \left[ \frac{T_s}{L_1} \right] \left[ \frac{d_1}{3} \right] \left[ \frac{\sqrt{V_o^2}}{3V_T} \right] $$

Then, by taking the average of (27) over a half-line period, its rms current stress is obtained as (28), shown at the bottom of the page, where $C = \cos(3\alpha) - \cos(3\beta)$.

Similarly, the current stresses on the other semiconductor devices can be calculated easily as
In addition, the voltage stresses on the semiconductor devices are stated in Table I.

D. Capacitors Optimization

To determine the size of the intermediate bus capacitor $C_B$, we can consider the hold-up time ($t_{\text{hold up}}$) of the circuit.

The bus capacitor $C$ will sustain all the output power within when the ac input source is removed. In normal practice, the hold-up time is one of the ac line cycle. In addition, the maximum capacitance of $C_B$ to meet this hold-up time requirement is determined under the low-line and full output load conditions. Thus, the size of $C_B$ is expressed as follows:

$$C_B = \left( \frac{V_B @ 90V_{\text{rms}}}{t_{\text{hold up}}} \right)^2.$$  \hfill (32)

Apart from the size of $C_B$, it is noted that the line frequency ripple on the output capacitor $C_o$ is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

E. Distribution of Direct Power Transfer

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_o (\theta) = p_{\text{PFC}} (\theta) + p_{\text{DC/DC}} (\theta)$$ \hfill (33)

where $p_o (\theta)$, $p_{\text{PFC}} (\theta)$, and $p_{\text{DC/DC}} (\theta)$ are denoted as instantaneous output power of the converter, output power of PFC cell and output power of dc/dc cell, respectively. Both instantaneous output powers of PFC and dc/dc cells can be calculated as
where pin and \( d_1(\theta) \) are defined as the instantaneous value of input power of the dc/dc cell and duty cycle \( d_1 \).

\( d_1(\theta) \) can be obtained easily once the average output current of the converter is determined. By concycle, the average output current of the converter is given by

\[
I_o = \frac{\int_0^T i(\theta)_{SW} \, d\theta}{T_{SW}} = \frac{d_1(\theta) t s}{T_{SW}}, \quad \alpha < \theta < \beta
\]

By substituting (37) into (34) and (35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the

**Fig. 6. Calculated power processing by PFC cell (red trace) and dc/dc cell (blue trace).**

**Condition:** \( P_o = 100 \, W \) (green trace), \( V_o = 19 \, V \) and \( M = 0.4 \).

Hence, \( d_1(\theta) \) in a half-line period is expressed as

\[
d_1(\theta) = \begin{cases} \frac{2P_o}{V_{in}(\theta) X_{dc} V_T}, & \alpha < \theta < \beta \\ \frac{2L_2 P_o}{V^2_{in}}, & \text{otherwise} \end{cases}
\]

By substituting (37) into (34) and (35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the
power proceed by PFC cell $p_{\text{PFC}}(\theta)$ and dc/dc cell $p_{\text{dc/dc}}(\theta)$, respectively. Besides, the green dash trace is the output power ($p_{\text{total}}(\theta)$) of the converter. It is noted that the power handled by both cells is changed oppositely to maintain the load power under different input voltages. At low-line condition, there is more input power coupled to the output directly. In contrast, more power is delivered to the output by the dc/dc cell at high-line condition. More discussion of the direct power transfer is given in Section V.

IV. EXPERIMENTAL RESULTS

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage ($<150\text{V}$) and high power factor ($>96\%$), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

### Table II

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC Controller</td>
<td>TL594</td>
</tr>
<tr>
<td>Input filter inductor $L_f$</td>
<td>2 mH</td>
</tr>
<tr>
<td>Input filter capacitor $C_f$</td>
<td>2 xF</td>
</tr>
<tr>
<td>Inductor $L_1$</td>
<td>106 xH</td>
</tr>
<tr>
<td>Inductor $L_2$</td>
<td>46 xH</td>
</tr>
<tr>
<td>Inductance Ratio ($M=L_2/L_1$)</td>
<td>0.434</td>
</tr>
<tr>
<td>MOSFET $S_1$</td>
<td>SPW47N60CFD</td>
</tr>
<tr>
<td>$D_1$</td>
<td>MUR3040PT</td>
</tr>
<tr>
<td>$D_2$</td>
<td>MUR3040PT</td>
</tr>
<tr>
<td>$D_3$</td>
<td>MUR3040PT</td>
</tr>
<tr>
<td>$C_p$</td>
<td>5 mF</td>
</tr>
</tbody>
</table>

Fig. 7. Measured input characteristic of the converter at (a) 90 Vrms and (b) 270 Vrms under 100-W condition

In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Section V. Taking the performance of the converter on bus voltage, power factor, and efficiency into account, the inductance ratio around $M = 0.4$ is selected. Table II depicts all the components used in the circuit, and its specification is stated as follows:

1) output power: 100 W;
2) output voltage: 19 Vdc;
Fig. 8. Comparison of IEC61000-3-2 Class D standard with measured input current harmonics at 270 Vrms.

Fig. 9. Measured output voltage (upper trace −10 V/div) and intermediate bus voltage (bottom trace −40 V/div) at (a) 90 Vrms and (b) 270 Vrms under full load condition.

3) power factor: > 96%;

4) intermediate bus voltage: < 150V;

5) line input voltage: 90–270 Vrms /50 Hz;

6) switching frequency ($f_s$): 20 kHz.

Fig. 7 shows the waveforms of the line-input voltage along with its current under full load condition at 90 Vrms and 270 Vrms, respectively. The measured current harmonics met the IEC61000-3-2 class D standard as shown in Fig. 8. In addition, the measured output and bus voltages under both low and high line conditions are shown as in Fig. 9. It can be seen that the bus voltage was kept at 123 V and well below 150 V at high-line condition. Fig. 10 illustrates the conversion efficiency of the proposed converter under different line input and output power conditions. The maximum efficiency of the circuit is around 89% at low line application. Furthermore, Fig. 11 shows the predicted intermediate bus voltage is in good agreement with the measured value.
V. DISCUSSION

According to [13] and [21], the direct power transfer ratio \( n \) under this type of capacitive coupling is \( \frac{V_o}{VT} \). It can be seen that the portion of direct power transfer from input to output decreases when \( VB \) becomes larger resulting in increase of \( VT \). In other words, the direct power transfer decreases when the line input voltage increases. It matches with the discussion in Section III-E. In addition, the increase of \( VB \) will lower the conversion efficiency of dc/dc cell due to larger voltage conversion around ten times at high-line condition, from \( VB = 123 \text{ V} \) down to \( V_o = 19 \text{ V} \). As a result, it further impairs the efficiency of the converter at high-line operation. On the other hand, from (2), decrease of \( VB \) extends the conduction angle of the converter leading to higher power factor. However, lower \( VB \) requires decrease of inductance ratio resulting in higher peak inductor currents and causing higher conduction loss. Thus, tradeoff has to be made for selecting the inductance ratio.
among the peak current of both inductors, bus voltage, and power factor. Nevertheless, the converter is capable to be used under high-line condition with the full load efficiency around 84% at 240 Vrms.

To continue with the comparison from Section I, Table III shows the performances of recent topologies and the proposed converter in more detail. In order to achieve low output voltage and low intermediate bus voltage with high efficiency for universal line operation, the topologies employ different approaches. Furthermore, every converter has their best performance when working at particular input and output conditions. Although the input and output conditions for the converters in the table are not the same, we have two criteria to compare their performances. First, for a given power level, the lower the output voltage of the converter, the lower the efficiency it gets due to more current flowing in the circuit. Second, for PWM converters, the fewer semiconductor devices used in the converter, the lesser the conduction and switching loss of the converter will be. However, the operational parameters, selection of switching frequency, and semiconductor will also impact on the circuit efficiency. Therefore, it is hard to have a fair efficiency comparison and, hence, circuit efficiencies shown are just for the information purpose. Nevertheless, apart from the efficiency, the performances on reducing the bus voltage, the step-down ratio and circuit complexity are less dependent on the input and output conditions, and operational parameters, but the topology itself and the inductance ratio. From the table and excluding all the isolated converters, it can be seen that the proposed converter is able to achieve the lowest bus voltage at high-line condition with low output voltage and probably higher efficiency among all transformerless topologies and its structure is simpler. In addition, comparing with [10], [18] at low-line condition, the proposed converter is also able to achieve the lowest bus voltage at around 33.5 V with positive output voltage and probably higher efficiency. Thus, the proposed converter has better performance for lower output voltage operation.

VI. CONCLUSION

The proposed IBuBuBo single-stage ac/dc converter has been experimentally verified, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150 V at all input and output conditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of trans-former, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protection. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency around 89%.
REFERENCES


**Shu-Kong Ki** (S’09) received the B.Eng. (Hons.) degree in electronic and information engineering from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2006. He is currently working toward the Ph.D. degree at The University of Sydney, NSW, Australia.

In 2005, he was a Research Technical Assistant at The Hong Kong Polytechnic University in electronic and information engineering. From 2007 to 2008, he was a Project Assistant with electrical department at the same university. His research interests include power electronics applications, LED lighting, energy saving, sustainable energy system, and CAD design of analog circuit.

**Dylan Dah-Chuan Lu** (S’00–M’04–SM’92) received the B.Eng. (Hons.) and the Ph.D. degrees in electronic and information engineering from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 1999 and 2004, respectively.

In 2003, he joined PowereLab Ltd. as a Senior Engineer. His major responsibilities include project development and management, circuit design, and contribution of research in the area of power electronics. In 2006, he joined the School of Electrical and Information Engineering, The University of Sydney, NSW, Australia, where he is currently a Senior Lecturer. He is a Member of the Editorial Board of Smart Grid and Renewable Energy, a Member of the Editorial Board of Energy and Power Engineering, and an Associate Editor of the Australian Journal of Electrical and Electronic Engineering. He has two patents on efficient power conversion. His current research interests include power electronic circuits and control for efficient power conversion, lighting, renewable electrical energy systems, microgrid and power quality improvement, and engineering education. He has published over 80 technical papers in the areas of power electronics and engineering education. Dr. Lu received the Dean’s Research Award in 2011 and is also a member of the Institute of Engineers Australia.