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IMPLEMENTATION OF A TURBO CODE USING LOG-MAP DECODER

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ABSTRACT

Turbo code is a great achievement in the field communication system. It can be created by concatenation of turbo encoder and decoder serially. Turbo encoder is build with parallel concatenation of two simple convolutional codes. It gives near Shannon capacity performance with applying in transmission system. We can make different configuration of Turbo encoder by varying number of memory elements. Turbo code also consist an interleaver unit which is the cause of delay but provide good performance. We can also generate a system according to rate, mostly we use rate 1/2 and 1/3. By puncturing method we can vary the rate. Turbo Decoder can be implemented using different algorithm, but using Log Maximum a posteriori (MAP) algorithm we can implement system with less complexity and good performance. Turbo encoder is designed and simulated using MATLAB. The implemented model of turbo code system is compared and verified with MATLAB.

Keywords: Turbo code, Shannon capacity, Interleaver, Puncturing, Code rate, Log map algorithm, MATLAB.

I. INTRODUCTION

Turbo-codes have received considerable attention and came in existence in 1993. It was proposed by berrou et al. Due to its powerful error correcting capability, reasonable complexity, and flexibility in terms of different block lengths and code rates, number of memory element etc. The turbo encoder consists two recursive systematic convolutional (RSC) encoders operating in parallel manner with the input data bits, we can design either of 4-state or 8-state turbo encoder, with different rate. An interleaver is used between two systematic convolution encoder as shown in Figure1. Here we get the rate 1/3 without puncturing and 1/2 with puncturing method. Other code rates are also obtained by puncturing mechanism.

Turbo encoded data is applied to turbo decoder through BPSK transmission over AWGN channel. Importantly, by applying these data to the Log-Map decoding structure provide performance nearer to Shannon capacity with feasible complexity. Turbo code are widely used in different communication system like satellite communication, CDMA, mobile communication etc.

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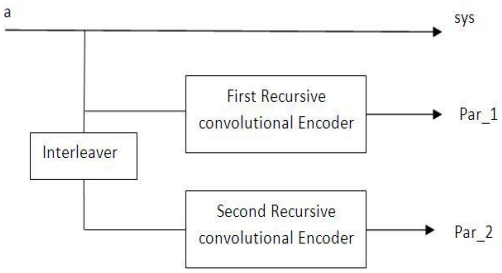

Fig. 1.1: Turbo encoder without puncturing (Rate 1/3)

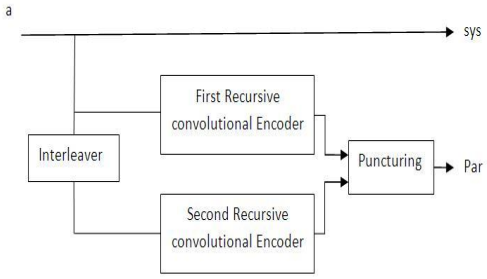

Fig. 1.2: Turbo encoder with puncturing (Rate 1/2)

For the implementation of turbo decoder first consideration is to select a SISO algorithm, which can give efficient performance. We chosen here Log-Map algorithm which provide good performance with less complexity.

In this paper, we first discuss about the turbo encoder and the variation on encoder with the implementation issue. Then we discuss about turbo decoder (SISO) algorithm. Then after we will show comparison and verification of the results obtained from implemented model using MATLAB.

II. LITERATURE REVIEW

Robertson P et al (1997) presented a comparison between log-MAP, max-log MAP and soft output Viterbi algorithm (SOVA) [3]. The comparison shows that SOVA is 0.7dB inferior to log-MAP and max-log-MAP lying in between SOVA and log-MAP. The comparative analysis is done for these algorithms in terms of number of additions, multiplication and look-up tables.

Gross W.J et al (1998) developed a simplified MAP algorithm suitable for the implementation of turbo decoder [4]. The simplification eliminates the need for a ROM or multiplexor-tree lookup table and replaces it with a constant value. The results show that the performance of turbo decoders is not adversely affected by this simplification.

Worm A et al (2000) presents a VLSI high speed MAP architecture with optimized memory size and power consumption for decoding the turbo codes [5]. The log-MAP and max log-MAP algorithm is used. Memory size is reduced by minimizing the FIFO memory size. For maximum throughput a fully pipelined architecture is considered. The area decreases by up to 11% and power consumption by up to 15% in case of a Log-MAP decoder and for a Max Log-MAP decoder, even an 18% area decrease and a 20% power decrease.

Wang Z (2002) introduced a variety of area efficient parallel turbo decoding schemes [6].Turbo decoders inherently have large decoding latency and low throughput because of iterative decoding. To reduce the latency and increase the throughput, high-speed decoding schemes are employed. So for that techniques like segmented

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sliding window approach and two other area-efficient parallel turbo decoding schemes .Comparison on storage requirements, number of computation units, and overall decoding schemes are made. Also in order to reduce the storage bottleneck partial storage of state metrics approach is also presented.

In 2003, Elassal M et al proposed a method to decrease the power consumption of turbo decoder [7]. In turbo decoder, decoding is done by iteratively exchanging the extrinsic information. In this proposed method the iteration is terminated when the extrinsic information exceeds a particular threshold and then a predefined value is terminated.

This reduced memory access for inter leaver and state metrics and thus power was reduced. 25% reduction of power consumption with energy per bit to noise power spectral density ratio Eb/No= 1.5 dB is achieved compared to conventional architecture.

Kwak J et al (2003) designed VLSI architecture for an efficient turbo decoder with parallel architecture to achieve high-throughput [8]. For 100% processing element utilization, a dividable interleaving method is proposed, in which it not only solves the memory conflict problem in extrinsic information memory, but also reduces the memory required for interleaver. It mainly consists of parallel decoding architecture using block partition method by maintaining the superior BER performance of MAP-based decoder.

Elmasry M et al (2004) designed rate 1/3, 8-state log-MAP turbo decoder architecture [9]. The simplified log-MAP algorithm is used for the component soft-in soft-out decoder (SISO). Several logic and architectural level techniques are applied through the design process to reduce power consumption, area and increase throughput of the turbo decoder Parallelism, quantization, resource sharing, logic reduction and normalization are applied to reduce area, power and throughput. 0.18µ CMOS technology is used [9]. The developed turbo decoder has a core area of 0.6mm2, clock frequency of 100MHz, power consumption of 63mW and energy efficiency of 2.5n J/b/iteration.

Tiwari M et al (2005) proposed the sliding window approach as a means for reducing memory requirements and decoding latency of MAP based SISO decoder [10].Optimal single-port memory sub-banking structure that supports very high throughput and low SISO decoding latency for a given sliding window configuration presented. The contributions include derivation of the optimal memory sub-banked structure for different SW (sliding window) configurations, also the study of the relationship between memory size and the energy consumption for different SW configurations and study of the effect of number of sub-banks on the throughput/decoding latency for a given SW configuration.

Atluri I et al (2005) formulated the implementation of a low power Log-MAP decoder with reduced storage requirement and based on the optimized MAP algorithm that calculates the reverse state metrics in the forward recursive manner [11]. The new low power derivatives of this decoder through a variation in the percentage of memory savings are presented. Three low power architectures of the Log-MAP decoder not employing the sliding window technique have been developed and post layout power savings of approximately 44%, 40% and 36% with respect to the conventional implementation have been observed.

III. PROPOSED APPROACH

We have implemented different configuration of turbo encoder. We vary the number of memory element and get the verity of structures, some of given below:

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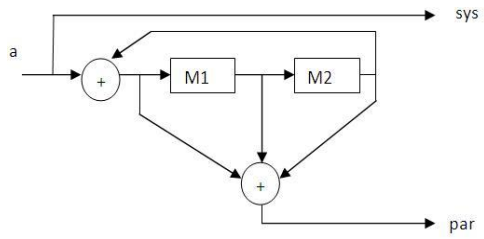
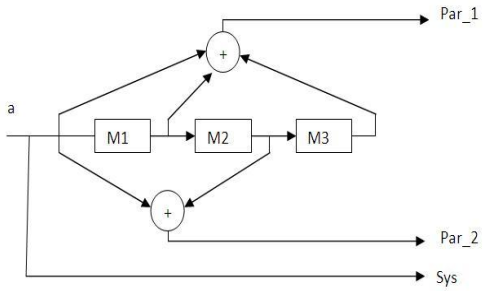
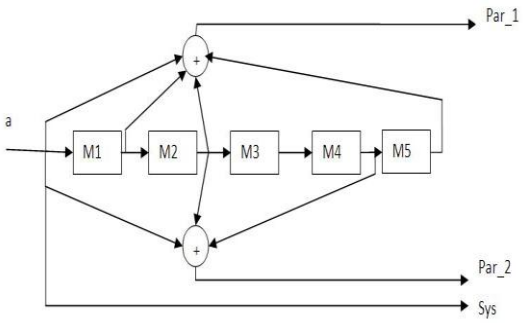
There are some of the following encoder structure that we have implemented namely (a), (b) & (c).



(3.1)



(3.2)



(33)

Fig. 3: (3.1) conf. (5, 7), (3.2) conf. (15, 12, 0), (3.3) conf. (71, 52, 0)

These configurations are used as in form of binary polynomial, the first one is (101, 111), second one is (1111, 1010) and finally third one is (111001, 101010).

From the above structure we get the sys, par_1 and par_2 sequences. These are available in form of rate 1/3. After puncturing of par_1 and par_2, we get alternatively combined parity sequence.

After implementing the turbo encoder, output sequence obtained from encoder is passed through decoder.

From the encoder a large number of data is passed, here, as a sample we can take 100 bit input data and according to rate 1/3 we get 100 sys bits, 100 par_1 bits and 100 par_2 bits. To get rate 1/2 par_1 and par_2 bits will mixed alternatively.

3.1 INTERLEAVER

In turbo code interleaver is a random block that is used to rearrange the input data bits with no repetition.

Interleaver unit is used in both encoder and decoder part. At the encoder side it generates a block of data, whereas in decoder part it correlates the two SISO decoder and help to correct the error.

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3.2 TURBO DECODER

Turbo codes can be decoded by either an A posteriori probability (APP) method or maximum likelihood method. Turbo decoder consist two SISO decoder separated by interleaver and de-interleaver, as shown in figure4. Due to noise encoded output data bit may get corrupted and reach at the decoder input in the form of r0, r1 and r2 respectively.

The first SISO decoder takes as input the received information data bits sequence r0 and received parity sequence r1, which is generated by RSC encoder 1. The output data seq. from first SISO decoder is interleaved and goes as an input for second SISO decoder. The second SISO decoder takes as input r0 as received information bit sequence and r2 received parity sequence. From the second SISO decoder we get the final output data. To improve the performance of turbo code its output is de-interleaved and goes to first SISO decoder as an input. This whole process is also called as iterative decoding process.

After certain iteration the output of decoder stops further performance improvement. There are different decoding algorithms are available, we used Log-MAP decoding algorithm, which uses iterative decoding process.

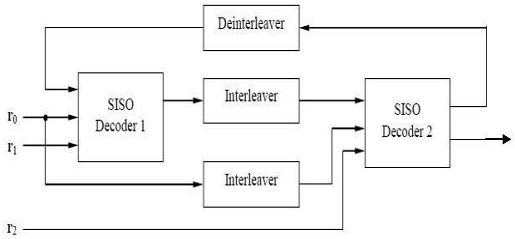

Fig. 3.2.1: General diagram of turbo Log MAP decoder

After getting output from both of the decoder, we take the soft decision here, we can also take hard decision as well but in case of soft decision performance is comparably better.

Finally, we calculate the BER (bit error performance) for certain set of signal to noise (Eb/No) ratio. According to BER curve we find the performance of system and comparison has done.

IV. RESULT

We take input data bits and finally obtained output data bits, and calculate BER (bit error rate). Now, with respect to signal to noise ratio (Eb / No), we plot the graph or it means we obtain the following Results:

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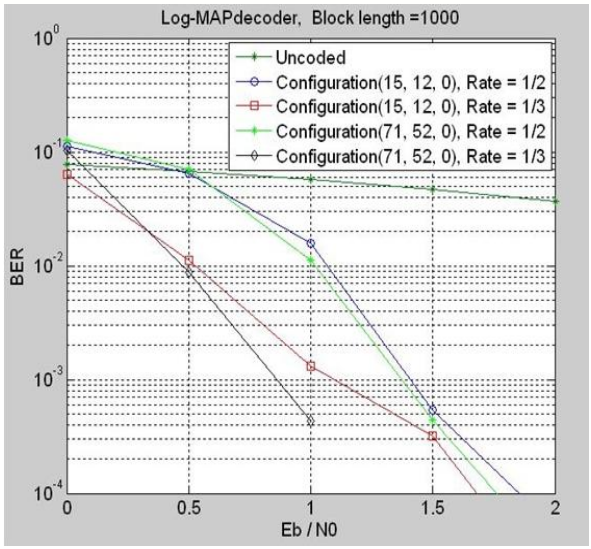

Fig. 4.1: Rate 1/2 vs Rate 1/3 for different configuration

From the above graph it is clear that if we go from rate 1/2 to rate 1/3, for any configuration of encoder, performance will comparatively improved. Here we check for two configuration of encoder first one is (15, 12, 0) and the second one is (71, 52, 0). In both of structure the above is satisfied.

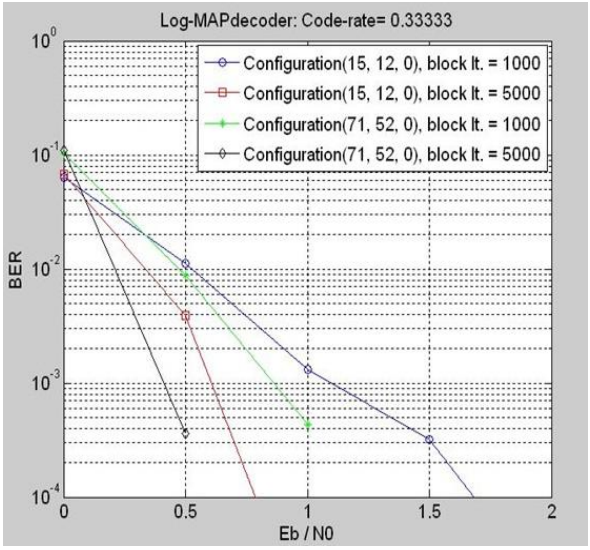

Fig. 4.2: performance comparison due to change in block length

From the above Figure7, it shown that if we change the block length size then this case performance will marginally improved, and here we conclude for given above two configurations and Rate 1/3.

Now, we will see the performance comparison due to change in number of memory element.

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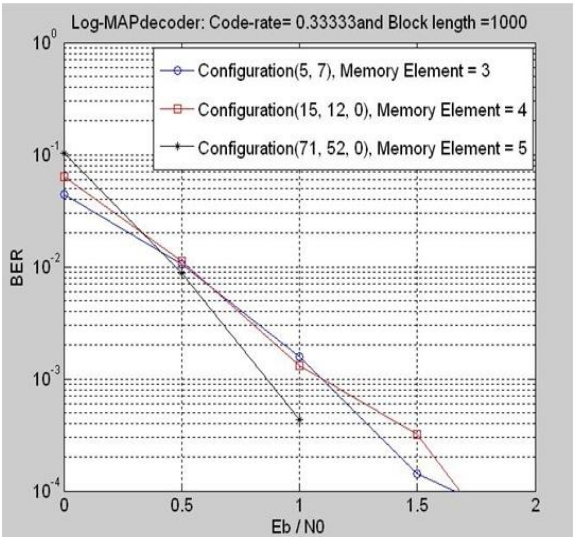

Fig. 4.3: performance comparison due change in memory element

From the above Figure7 it is clear that if choose higher number of memory elements in our encoder structure, improvement in performance occurs.

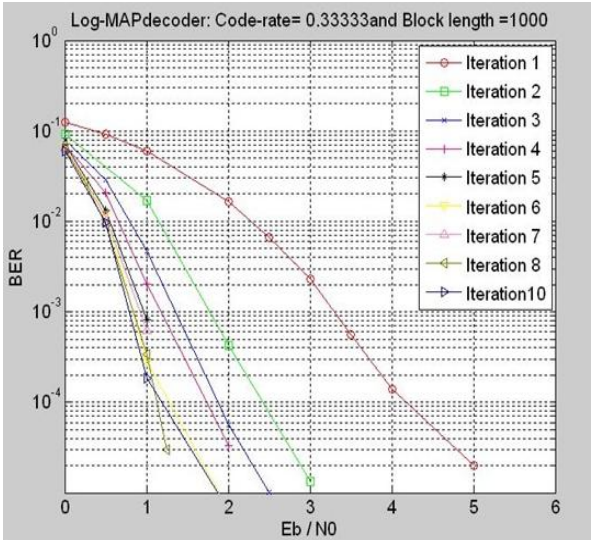

Fig. 4.4: Performance of turbo coding with Log MAP algorithm

From the above Figure8, it is clear that that we plotted the curve up to 10 iteration and we observe that when we go from 8 to 10 iterations, performance improvement not shown here, and curves are overlap each other.

V. COMPARISON AND VERIFICATION

We plotted the curve for Rate 1/2 and Rate 1/3, according to different configuration of turbo encoder. We have taken the following configuration of encoder (a) conf. (5, 7), (b) conf. (15, 12, 0) and (c) (71, 52, 0). We implemented and simulated these all with the help of MATLAB. In addition with this we also implemented Log MAP decoder using.

Finally we saw that all plots satisfy previous given trends of performance.

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VI. CONCLUSION

In this paper, a design of turbo encoder using MATLAB implemented turbo decoder is proposed and finally, performance comparison and Verification made the turbo code implementation. The obtained result shows that performance provides by Log MAP decoder is nearer to Shannon capacity. We have implemented turbo code using MATLAB with Log MAP turbo decoder. Finally comparison and verification is done. We have chosen this system for implementation because it reduces complexity up to certain level with less compromise in performance of turbo code, and it also improves the performance of communication system.

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