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Comparative Study of Efficient Fangled Viterbi Decoders

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ABSTRACT

Convolutional encoding with viterbi decoding is a good forward error correction technique suitable for channels affected by noise degradation. Fangled viterbi decoders are a variant of viterbi decoders which decodes quicker and takes less memory with no error detection capability. Modified fangled takes it a step further by gaining one bit error correction and detection capability at the cost of just double computational complexity and increase in memory requirement to 256 bits for 14 bit received data from constraint length 3 encoder. So a new method efficient fangled viterbi algorithm is proposed to deal with the increase in computational complexity and memory requirement with 1 bit error correction capability.

Keywords: constraint length, code rate, hamming distance, path metric, branch metric.

I. INTRODUCTION

In 1967 A.J. Viterbi [1] proposed viterbi algorithm for decoding convolutional codes. Viterbi decoding is a maximum likelihood method for decoding convolutional codes which attempts to reconstruct the action of convolutional encoder based on the trellis diagram. So it can construct the maximum likelihood path given the input sequence or it replicates the action of the convolutional encoder [7].

Viterbi decoders are used for small constraint length (K) convolutional codes i.e. K<=10 because of increase in decoders complexity with K [2]. Decoder complexity is in design as well as computational. Viterbi decoders have fixed decoding delay as a distinct advantage over sequential decoding algorithms [7]. Other parameters affecting the design of decoders are overall memory requirement, power consumption, area occupied and total cost of the design [5]. Each parameter is intertwined with each other thus can only be optimized with respect to application. Out of these optimization of memory requirement and computational complexity is dealt with in this paper.

Fangled viterbi decoder has least computational complexity, delay and memory requirement because it calculates only one path in the trellis diagram hence no error detection capability. Modified fangled can correct one bit error as it can calculate and compare both paths on emergence of error thus more memory and computations leading to delay [6]. Efficient fangled corrects error by taking decision on path selection in case of error leading to performance close to fangled Viterbi decoder.

Figure 1 shows trellis diagram for the paths corresponding to input sequence [11 10 10 11 01 01 11]. One bit error is introduced at sixth bit position or third symbol of the original sequence. The normal line is for output data bit ‘0’ and dashed line is for ‘1’. We have taken constraint length (K) =3 encoder, making four states in trellis. Dark line is used for correct path and ‘X’ is for wrong branch like branch 00 on the first frame. Other abbreviations are as follow:

- Received erroneous data (RED).

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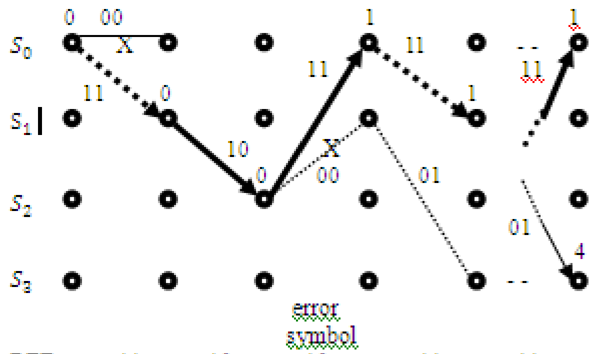
- Original data from encoder (OD).
- Original message to encoder (OM).
- Modified fangled decoder output (OM).
- Fangled decoder output (FO).



RED	11	10	10	11 -- -- 11
OD	11	10	11	11 -- -- 11
OM	1	0	0	1 --1 0- 0
MO	1	0	0	1 --1 0-- 0
FO	1	0	1	1 --0 1 -- 1

Figure 1. Trellis diagram of path followed by sequence [11 10 10 11 01 01 11] from K=3, R=1/2, (2, 1, 2) encoder.

The paper is organized as follows. Section 2 describes fangled viterbi decoding algorithm of convolutional codes, section 3 gives description of modified fangled viterbi algorithm, section 4 describes proposed efficient fangled viterbi decoding algorithm and section 5 concludes the paper.

II. FANGLED VITERBI DECODING ALGORITHM [3]-[4]

The flow chart for this algorithm is shown in Figure 2. Almost similar to conventional viterbi decoder this fangled decoder consists of following functional units [3].

- ❖ Encoder Engine
- ❖ Branch metric generator
- ❖ Add-Compare-Select unit (ACSU)

The encoder Engine replicates the Convolution encoder at the receiver and calculates the next state and the output for the various given states and inputs simultaneously as shown in table 1. As seen every state transition gives one output bit for respective input symbols i.e. reverse of encoder. The branch metric unit calculates the branch metrics by using hard decision based on hamming distance as it is easy to implement.

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Start State	Input Symbol	End State	Output Bit
00	00	00	0
00	11	01	1
01	10	10	0
01	01	01	1
10	11	00	1
10	00	01	0
11	01	10	1
11	10	11	0

Table 1. State and Output table for Viterbi Decoder.

An Add Compare Select unit (ACSU) receives two branch metrics and a path metric. It adds each incoming branch metric with the corresponding path metric and compares the two results to select the smaller one for updating the existing path metric as shown in figure 1. An ACS unit selects the associated survivor path decision.

As shown in Figure 1 no identifiable path is there for conflicts on third symbol as there is no guarantee that state transition will be from state 2 to state 0 (correct) or state 1 (incorrect) i.e. 10 to 00 (correct) or 11. So in case of an error when selector unit in the ACS finds itself in a dilemma of choosing among equal paths, makes an arbitrary branch selection (here branch 00) leading to serious unreliability of the data thus decoded.

Advantage of fangled can be seen in figure 1, for every symbol only one path is stored and two additions and one comparison are done. So for 14 bit received data i.e. 7 symbols only 14 add and 7 comparisons are done [4] and corresponding memory requirement for storing path and state metric, states and survivor as well as decoded data is 88 bits [6].

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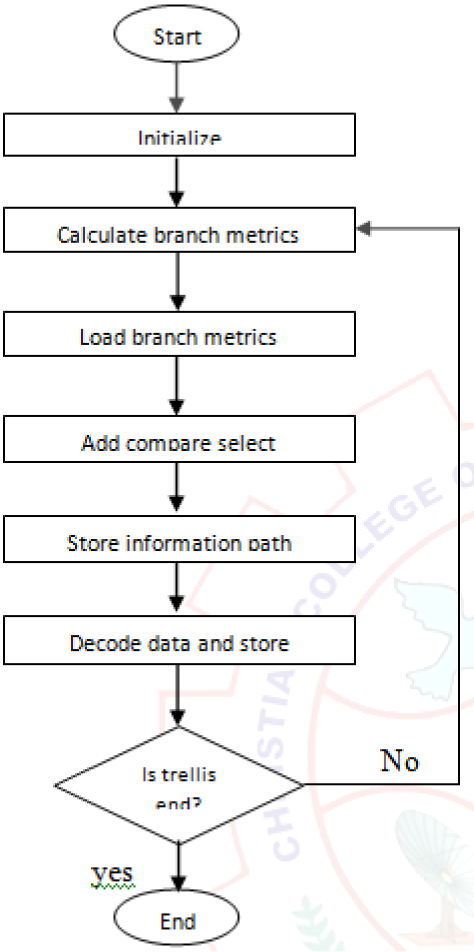

Figure 2. Fangled viterbi algorithm's flowchart

Disadvantage is no error detection capability in fangled method hence unreliable output [6].

III. MODIFIED FANGLED VITERBI ALGORITHM [6]

Modified Fangled Viterbi algorithm is a variant of fangled Viterbi algorithm designed to correct one bit errors [5]. Computational complexity and memory requirement is more than fangled but much lower than conventional Viterbi decoder. The main difference is that modified fangled takes both paths in case of a conflict or error and compares them at the end for the choice of optimum path [6] as shown in figure 3. Thus completely fails in case of noisy channel that can introduce burst error. The modified fangled decoder also has the same blocks as the fangled decoder:

- Branch metric and path metric memory
- Add compare select unit

Survivor memory

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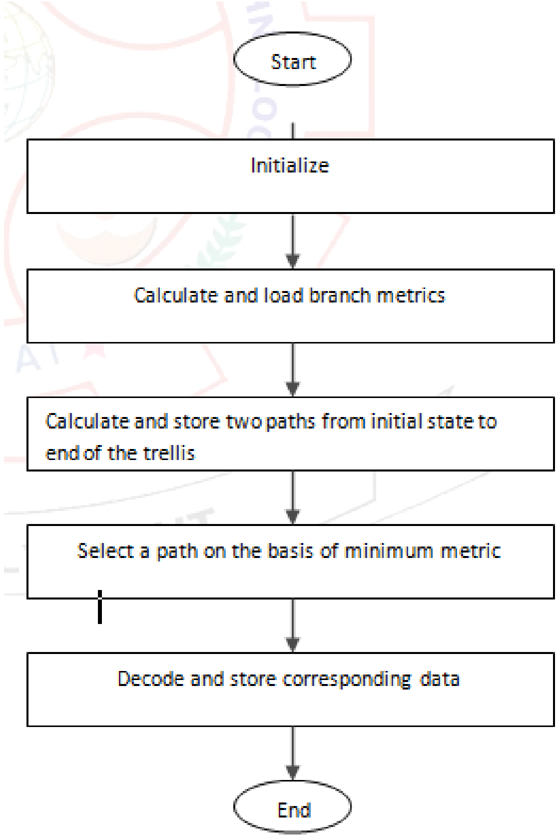

Figure 3. Modified Fangled Viterbi algorithm

If an error occurs in the received data as in third symbol shown in figure 1, then the branch metric unit of that error frame has two possible states 00 (correct) and 10 with equal metric, leading to a conflict of branch selection between 11 (correct) and 00. In fangled algorithm this conflicting situation is resolved by randomly selecting any path which leads to erroneous decoding of data [4]. But this miscalculation is solved in modified fangled algorithm by selecting both paths and calculating there total path metric from initial state to completion of trellis and storing the error metrics of each path which came as 1 and 4. Both paths are now compared and the minimum path with metric 1 is selected, consequently resolving the issue and giving error free data [1 0 0 1 1]. Note that for error free data both paths will coincide till the end.

Advantage of modified fangled algorithm is its 1 bit error correcting capability giving reliability to the decoder. But it carries the calculation of both the path metrics from the initial stage with and without error, even irrespective of the stage at which the conflict of branch selection or error occurs. Hence leading to 28 adds and 14 compares for 14 bit received data from K=3 encoder. The second path requires additional memory, enhancing memory requirement to 256 bits [6].

IV. EFFICIENT FANGLED VITERBI ALGORITHM:

As shown in the flowchart in figure 4, efficient fangled viterbi decoder is an extension of fangled and similar to modified fangled but its core is the decision unit. This removes the redundancies in modified fangled design like extra computations and consequent memory requirement.

The whole design can again be bifurcated into:

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- Encoder engine
- Branch metric calculation unit (BMU)
- Decision unit
- Survivor path calculation unit (SMU)

Encoder engine, BMU and SMU are same as explained in previous sections.

Decision Unit:

Decision unit works same as an ACSU in fangled Viterbi decoder on uncorrupted data. In case of an error it faces with the same challenge of finding the correct path. Throughout the paper it is assumed that one bit error can cause the path metric to increase by one. When such happens modified fangled used to calculate both path and compare them at the end [6]. Efficient fangled method does so by taking future symbol 11 from received data i.e. the very next two bits after error symbol to compute path metric for choosing correct path.

In figure 1, one bit error occurred at third symbol i.e. ‘10’ increasing the path metric from 0 to 1. Now fourth symbol i.e. ‘11’ is taken and path metric then calculated increases to 2. This leads to the conclusion that this path is wrong, as the correct path’s, path metric always increases to one for one bit error and remains the same thereafter. Hence further calculation of this path is terminated. As in case of modified fangled both paths coincide till error symbol in the trellis, so now the second pat can be calculated from symbol 3 whose path metric can be seen as 1 from figure 1 so it is the correct path.

Effective fangled algorithm gives a clear advantage over modified scheme as this takes extra computation of two branch metrics, their addition with path metric and one comparison operation. Considering the same for symbol 3 now extra 4 add and 2 compare means a total of 18 add and 9 compares for 14 bit received data. Extra memory of 11 bits for extra state transition and subsequent metric storage is required but the total memory requirement is yet to be analyzed. Efficient fangled method can also be developed for 2 bit error correction.

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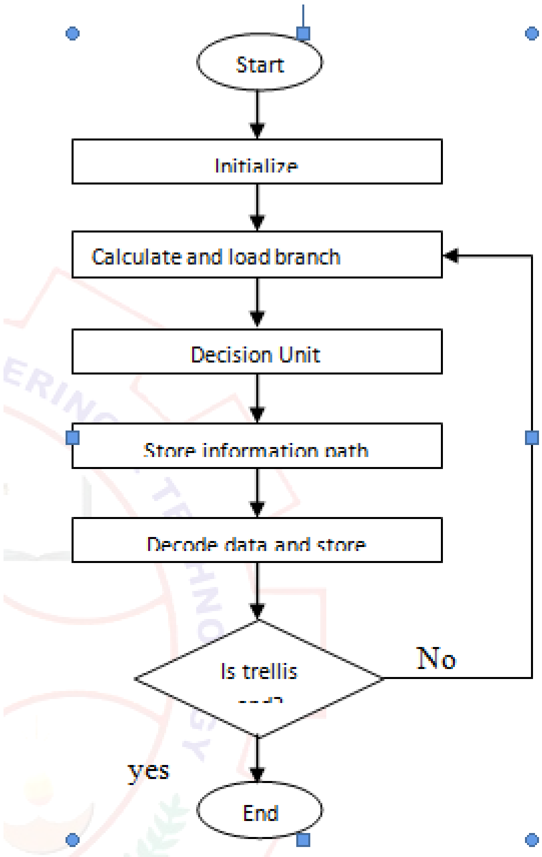

Figure 4. Efficient fangled viterbi algorithm's flowchart

Disadvantage is that it cannot correct burst error both bit and symbol wise. It takes 30% more computation than fangled viterbi decoder.

V. CONCLUSION

The modified method though can correct one bit error increases the other two parameters i.e. double computation complexity and memory requirement to 256 bits when compared to fangled method for 14 bit data from K=3 convolutional encoder. Efficient method manages to give better performance in computation complexity by 64% with respect to modified method with the same reliability. These methods can be applied where not channel noise degradation but resources and time delay are a constraint. Efficient fangled method can also be improved as modified fangled for burst error by using inter-leavers and de-inter-leavers [6].

REFERENCES

[1] A.J. Viterbi, "Error bounds for convolutional codes and an asymptotically optimum decoding algorithm"' *IEEE Trans. Inform. Theory*, vol. IT-13, pp.260–269, 1967.

[2] Hema. S, Suresh Babu V. and Ramesh P, "FPGA Implementation of Viterbi Decoder", Proceedings of the 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Greece, February 16-19, 2007.

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

[3] Rajaram Shivasubramaniam and Abhaikumar Varadhan, "An efficient implementation of IS-95A CDMA Transreceiver through FPGA", *DSP Journal*, Volume 6, Issue 1, September-2006.

[4] Syed Ubed Ur Rahman, Shivanand kulkarni and Sujatha C M, "An alternative scheme for Viterbi decoding of convolutional codes", NLPPES-2010, Bangalore.

[5] Shivanand Kulkarni, "Implementation of convolution- nal Viterbi decoder on FPGA and measuring its performance", MTech thesis in R.V.C.E., Bangalore, 2009-2010.

[6] Syed Ubed Ur Rahman, "Implementation of fangled Viterbi decoder on FPGA and measuring its performance", MTech thesis in R.V.C.E., Bangalore, 2009-2010.

[7] Shu Lin and Daniel J. Costello, Jr, "Error control coding: fundamentals and applications", Prentice hall of India, 3-e., 2005.