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LOW POWER CMOS CELL STRUCTURES BASED ON ADIABATIC SWITCHING

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ABSTRACT

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this paper, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

Keywords: Adiabatic logic, PFAL, energy dissipation

I. INTRODUCTION

There are various interpretations of the *Moore's Law* that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by *American Council for an Energy-Efficient Economy* estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend.

II. SOURCES OF POWER DISSIPATION

Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic

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(TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI). The power consumed when the CMOS circuit is in use can be decomposed into two basic classes: static and dynamic.

The static or steady state power dissipation of a circuit is expressed by the following relation [1]

$$P_{stat} = I_{stat} V_{DD}$$

where, I_{stat} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from V_{DD} to ground as PMOS and NMOS transistors are never on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation. For a sub-micron NMOS device W/L = 10/ 0.5, the substrate injection current is of the order of 1- 100 μA for a V_{DD} of 5 V [2]. Another form of static power dissipation occurs for the so-called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic family. In this, the PMOS pull-up is always on and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from V_{DD} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of the strength of PMOS and NMOS networks hence the name. The static power consumed by these logic families can be considerable. For this reason, logic families such as this, which experience static power consumption, should be avoided for low-power design. With that in mind, the static component of power consumption in low-power CMOS circuits should be negligible and the focus shifts primarily to dynamic power consumption.

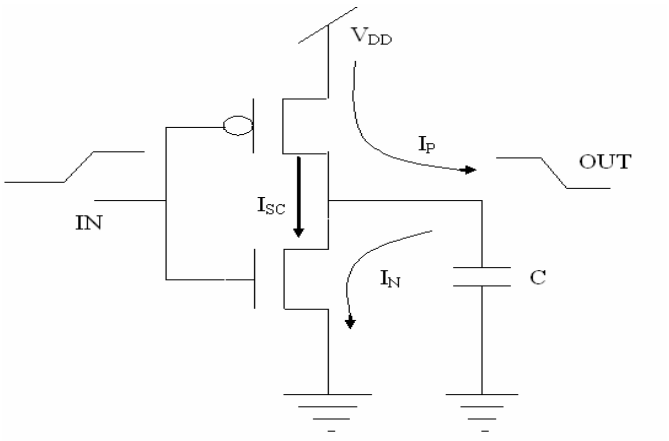

Fig. 1. CMOS Inverter for Power Analysis

III. DYNAMIC POWER

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between V_{tn} and V_{DD} - V_{tp}. During this time, a short-circuit exists between V_{DD} and ground and the currents are allowed to flow. A detailed analysis of this phenomenon by Veendrick reveals that with careful design of the transition edges, this component can be kept below 10-15% of the total power [2]; this can be

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achieved by keeping the rise and fall times of all the signals throughout the design within a fixed range (preferably equal). Thus, although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation due to capacitance charging consumes most of the power. This component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit. The situation is modelled in Figure 2.1, where the parasitic capacitances are lumped at the output in the capacitor *C*. Consider the behaviour of the circuit over one full cycle of operation with the input voltage going from V_{DD} to ground and back to V_{DD} again. As the input switches from high to low, the NMOS pull-down network is cut-off and PMOS pull-up network is activated charging load capacitance *C* up to V_{DD}. This charging process draws energy equal to CV_{DD}^{2} from the power supply. Half of this is dissipated immediately in the PMOS transistors, while the other half is stored on the load capacitance. Then, when the input returns to V_{DD}, the process is reversed and the capacitance is discharged, its energy being in the NMOS network. In summary, every time a capacitive node switches from ground to V_{DD} (and back to ground), energy of CV_{DD}^{2} is consumed.

This leads to the conclusion that CMOS power consumption depends on the *switching activity* of the signals involved. We can define *activity*, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, *f*, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: αf. This leads to the following formulation for the average CMOS power consumption:

$$P_{dyn} = \alpha C V_{DD}^{2} f$$

This classical result illustrates that the dynamic power is proportional to the switching activity, capacitive loading and the square of the supply voltage. In CMOS circuits, this component of power dissipation is by far the most important accounting for at least 90% of the total power dissipation [2].

So, to reduce the power dissipation, the circuit designer can minimize the switching event, decrease the node capacitance, reduce the voltage swing or apply a combination of these methods. Yet, in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply.

IV. ADIABATIC SWITCHING

A novel class of logic circuits called ADIABATIC LOGIC offers the possibility of further reducing the energy dissipated during the switching events and the possibility of recycling or reusing some of the energy drawn from the power supply [3]. To accomplish this goal, the circuit topology and the operating principle have to be modified, sometimes drastically. The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed and the voltage swing.

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-

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life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS* [3].

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

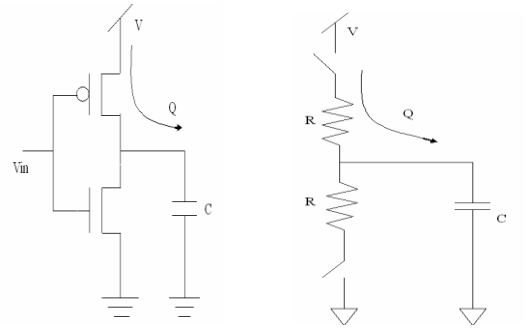

Figure 2. (a&b)

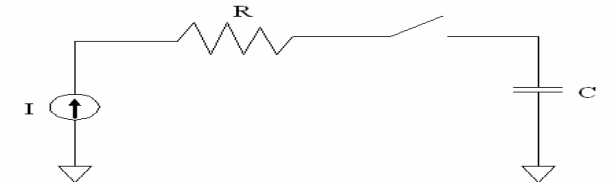

Figure 3. Circuit explaining Adiabatic Switching.

Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, *R* is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage V_C is zero initially [9].

∴ The voltage across the switch = *IR*

P(t) in the switch = $I^2 R$

∴Energy during charge = $(I^2 R)\, T$ (1)

Also I= CV/T =>T= CV/I (2)

$$E = (I^2R)T = \left(\frac{CV}{T}\right)^2 RT = \frac{C^2\ V^2}{T} R \quad (3)$$

$$\text{Hence } E = E_{diss} = \frac{RC}{T}(CV^2) = \frac{2RC}{T}\left(\frac{1}{2}CV^2\right) \quad (4)$$

Now, a number of observations can be made based on Equation (3.3) as follows:

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(i) The dissipated energy is smaller than for the conventional case, if the charging time *T* is larger than *2RC*. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,

(ii) Also, the dissipated energy is proportional to *R*, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

Let us examine simple circuit configurations which can be used for adiabatic switching. Figure 2(b) shows a general circuit topology for the conventional CMOS gates and adiabatic counterparts. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node.

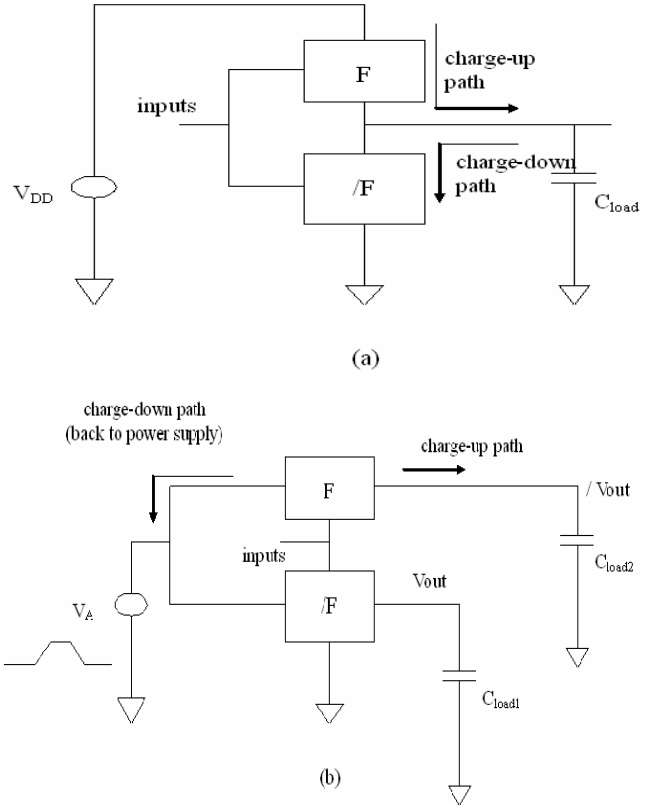

Figure 4 (a) The general circuit topology of a conventional CMOS Logic Gate.(b) The topology of an Adiabatic Logic Gate implementing the same function. Note the difference in charge-up and charge-down paths for the output capacitance

Note that all the inputs should also be available in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output. Note the circuit modifications which are necessary to convert a conventional CMOS logic circuit into an adiabatic logic circuit increase the device count by a factor of two or even more [6].

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V. ADIABATIC COMPUTING

The energy CV_{DD}^2, which is consumed in the conventional CMOS circuits, is unavoidable since the charge is transferred from the supply and returned to the ground [9]. The current drawn from the supply during a $0 \rightarrow 1$ transition is relatively large because of the large drain-source voltage. If, however, the supply voltage can be varied in a manner that would reduce the drain current, the energy will be significantly reduced. This can be achieved by using adiabatic circuits. Consider the circuit shown in the Figure 3.3. This circuit is sometimes refereed to as a pulse power supply CMOS (or PPS CMOS) [9].

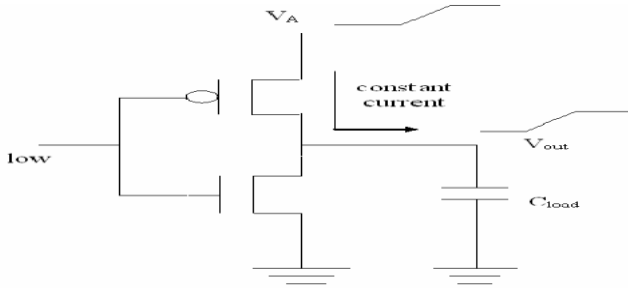

Figure 5. Schematic of (Adiabatic) PPS CMOS Inverter [9].

Its topology is very similar to that of the conventional CMOS inverter, except that its supply is driven with a pulsed supply waveform ω. Let us assume, the input is low and that the output (*out*) was initially low. With the V_{DD} being low, the drain current = 0. Now, as the voltage supply V_{DD} ramps up, the output follows the supply voltage V_{DD}.

The drain-to-source voltage is always small and so is the current drawn from the supply. The adiabatic logic circuit is also known as PULSED POWER SUPPLY (PPS) CMOS.

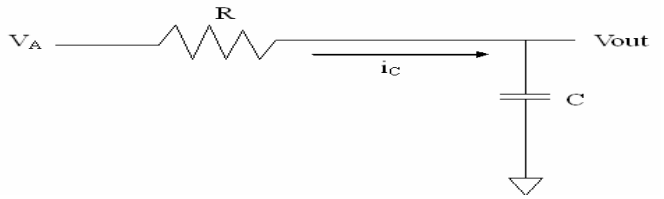

Figure. 6. The RC model of PPS CMOS Inverter.

Assume that the supply is increasing in steps from 0 to V_{DD}. Let us first derive the energy per step as follows [10] ⇒

Between the i^{th}-step and the next one, the supply voltage changes from V_i to V_{i+1}.

$$I_D = I = C\frac{dv_0^2}{dt} = \left(\frac{V_{i+1}-V_0}{R}\right) \qquad (5)$$

Solving this differential equation from $t = t_i$ (when the supply switches to V_{i+1}) to any time $t < t_{i+1}$, we get the following expression for the output voltage as a function of time.

$$V_0 = V_{i+1} - \left(\frac{V_{DD}}{n}e^{-t/RC}\right) \qquad (6)$$

Here, n is the number of step supply voltage.

Now, substitute from Equation (3.20) into Equation (3.19), we obtain the current expression, which is then used for the derivation of the energy consumed per step

$$E_{step} = \int_0^\infty I^2 R dt = \int_0^\infty \left(\frac{V_{DD}}{nR}e^{-t/RC}\right)^2 Rdt \qquad (7)$$

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$$E_{step} = \frac{1}{n^2}\left(\frac{1}{2}CV_{DD}^2\right) \quad (8)$$

Thus, the energy consumed for one operation in *nEstep*.

∴ Theoretically, if *n* is infinite (i.e., the *VDD* is a slow ramp), the energy goes to zero.

$$E_{total} = nEstep \quad = \left(\frac{1}{n^2}\right)\left(\frac{1}{2}CV^2\right) \quad (9)$$

The PPS-CMOS can be used for the complex Boolean function implementation.

Hence, the adiabatic circuits are operable only much lesser speeds comparable to SCMOS circuits. Another disadvantage is the requirement of a special type of power supply.

A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Just losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

Each different implementation of adiabatic logic shows some particular advantages, but there are also some basic drawbacks for these circuits. Let's see the details about each of these.

VI. DESIGN AND POWER DISSIPATION ANALYSIS OF LOW POWER CMOS CELL STRUCTURES

All the design structures based on CMOS Logic and Adiabatic Switching Logic are designed and simulated using standard TSMC 0.35 *μm* CMOS technology and 3.3 V voltage supply at an operating temperature of 27º C. Mentor Graphics Corporation based tool known as IC Design Architect have been used for all the design and analysis. The basic cells, for example, Inverter, Two-Input NAND Gate, Two-Input NOR Gate, Two-Input Exclusive-OR Gate, Two-to-One Multiplexer, One-Bit Full Adder are designed and analyzed with appropriate sizing. The SPICE BSIM 3v3 Version 3.1 MOS Model parameters

a. DESIGN AND SIMULAT FOR A CMOS INVERTER

The first basic cell which the VLSI designers implements and analyze is the basic CMOS Inverter. Here also this thesis work starts with the designing of the basic CMOS Inverter of minimum transistor size. The standard TSMC 0.35 *μm* CMOS technologies have been used and a load capacitance of 4 *fF* is used. The transient analysis is done by use of the ELDO Simulator of Mentor Graphics Corporation. The basic structure of a CMOS Inverter is shown in Figure 5.1

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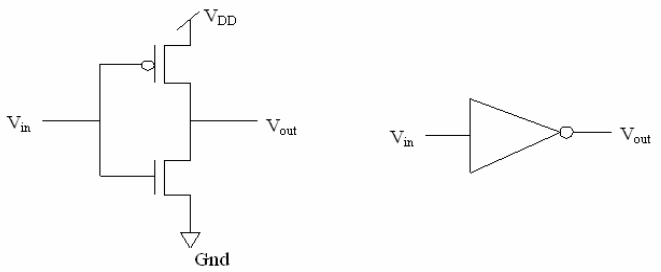

Figure 7. The Basic Structure of CMOS Inverter

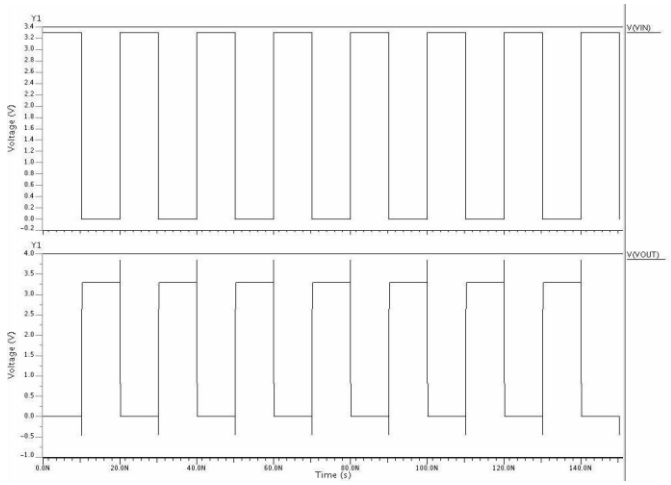

Figure 8 Simulation Results of CMOS Inverter:

(a) Input Signal, (b) Voltage Waveform of Output Signal.

b. POWER DISSIPATION ANALYSIS WITH FREQUENCY

This section deals with the comparison of the full complementary CMOS logic style with the ultra low-power adiabatic logic style in terms of the average dynamic power dissipation, expressed in micro-Watts.

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	1.4752 µ	0.1249 µ
50 M	2.9497 µ	0.2820 µ
100 M	5.8979 µ	1.3681 µ
125 M	7.2918 µ	1.7383 µ
150 M	8.8989 µ	3.2294 µ
200 M	11.7937 µ	8.3552 µ
250 M	14.5424 µ	12.5624 µ

TABLE 1.1

Average dynamic power dissipated by static CMOS family and adiabatic PFAL family for an inverter for different power clock frequencies

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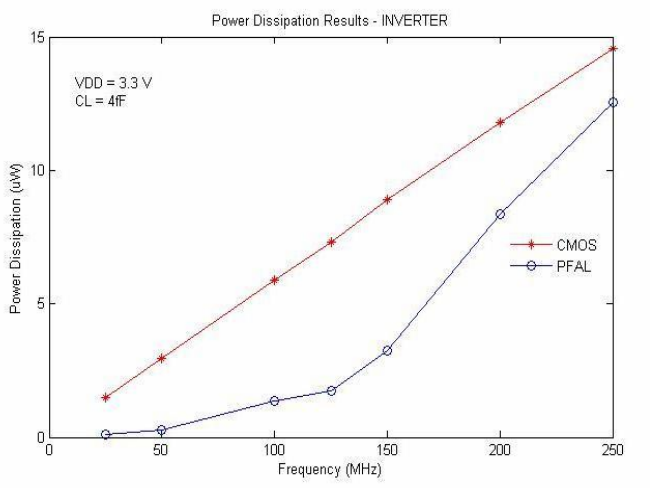

Figure 9. Power Dissipation Results for Two-Input NAND Gate.

DESIGN AND SIMULATION FOR A TWO-INPUT CMOS NAND GATE

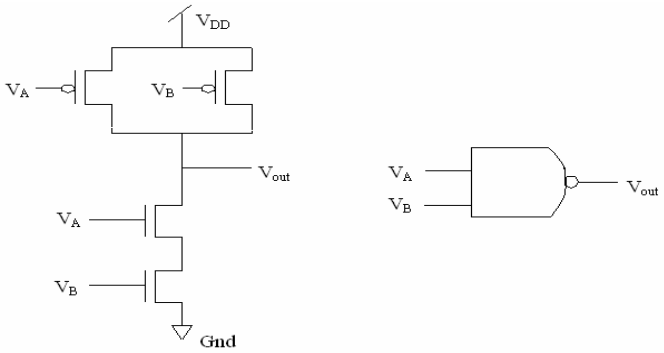

Figure 10. The Basic Structure of a Two-Input CMOS NAND Gate.

The next basic cell to consider is the CMOS-based Two-Input NAND Gate, designed and simulated in the standard TSMC 0.35 μm CMOS Technology and with a load capacitance of 5 fF. The minimum sized NMOS and PMOS transistors have been used for the transient simulations.

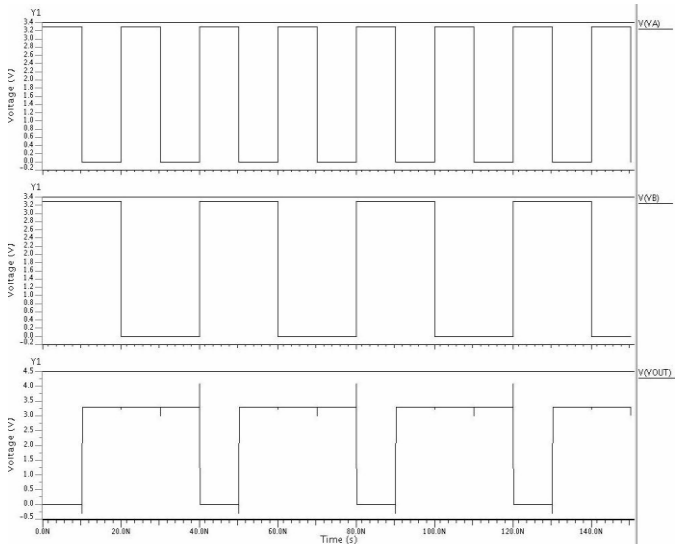

Figure 11. Simulation Results of Two-Input CMOS NAND Gate:

(a) Input Signal (VA), (b) Input Signal (VB),

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(c) Voltage Waveform of Output Signal (NAND Output).

Frequency (MHz)	Static CMOS (μW)	Adiabatic (PFAL) Logic (μW)
25 M	5.5229 μ	0.1032 μ
50 M	11.0486 μ	0.1897 μ
100 M	21.9064 μ	0.3575 μ
125 M	27.3754 μ	0.4432 μ
150 M	33.0029 μ	0.4857 μ
200 M	43.9415 μ	0.8198 μ
250 M	54.8195 μ	1.8702 μ

TABLE 1.2

Average dynamic power dissipated by static CMOS family and adiabatic PFAL family for two- input nor gate for different power clock frequencies

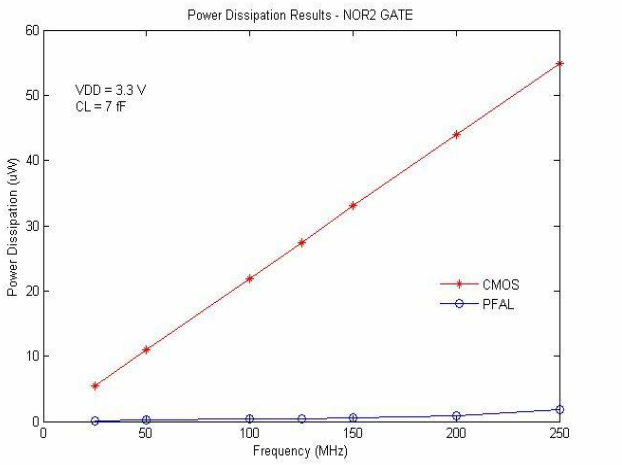

Figure 5.28. Power Dissipation Results for Two-Input NOR Gate.

VII. CONCLUSIONS

The paper focus on the design of low power CMOS cell structures. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic PFAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

A family of full-custom conventional CMOS Logic and an Adiabatic Logic units were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 *μm* technology, layout them in Mentor Graphics IC Station and the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done. It was found that the adiabatic PFAL logic style is advantageous in applications where

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power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants.

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