

Analysis and Design of MOS Current Mode Logic Circuits with Passive Inductor Load

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ABSTRACT

In this paper, the analysis and design of an improved version of conventional MOS current mode logic (MCML) also known as the shunt-peaked MCML style is presented. This logic style employs inductors in the load. The analytical formulation of the shunt-peaked MCML (MCML-SP) inverter employing the spiral is put forward. A design approach for shunt-peaked MCML inverter is also developed which can easily be extended for shunt-peaked digital circuits. The performance of the designed circuits is compared with their respective MCML counterparts through simulations using TSMC 0.18 μm CMOS technology parameters. A maximum delay reduction of 29 % is achieved for shunt-peaked MCML circuits. The impact of process variation on the MCML-SP and conventional MCML inverter at different design corners shows similar variations.

Keywords: Digital circuits, High-speed, MCML, Mixed signal ICs, spiral inductor, high-speed

I. INTRODUCTION

The recent advancements in the VLSI technology have led to the development of high-resolution mixed-signal applications. These applications demands high performance digital circuits to be integrated with analog circuitry on the same chip. MOS current mode logic (MCML) style has been widely used to design of digital circuits for mixed-signal applications as they provide an analog friendly environment due to the low switching noise [1-6].

An improved version of the conventional MCML logic style named as shunt-peaked MCML logic style has been suggested in literature [7, 8]. This logic style is based on the technique of shunt-peaking and involves the use of inductors. A variety of digital circuits based on the shunt-peaked MCML logic style has been suggested [8-10]. However, the detailed analysis and the design of the shunt-peaked MCML circuits are not presented in any of them. In this paper, the design of shunt-peaked MCML circuits through analytical modeling is put forward.

The paper first presents an overview of the conventional MCML style in section 2. Then, the analysis of the shunt-peaked MOS current mode logic style employing spiral inductors is presented in section 3. An approach to design shunt-peaked MCML inverter is formulated in section 4 which is extended for shunt-peaked digital circuits. A variety of digital circuits is designed and is compared with the conventional MCML counterparts through simulations using 0.18 μm TSMC CMOS technology parameters in section 5. The impact of process variation at different design corners is also studied. Finally section 6 concludes the paper.

II. MOS CURRENT MODE LOGIC (MCML) STYLE

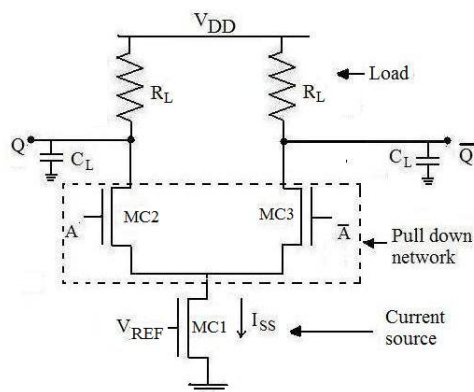
A conventional MCML circuit consists of three main parts: a pull-down network (PDN), a constant current source, and a load circuit. The PDN implements the logic function by applying the series-gating approach [4]. The constant current source MC1 provides the bias current I_{SS} while the load resistor R_L determines the voltage swing. A schematic of a conventional MCML inverter with differential input A is shown in Fig.1. It works on the principle of current steering. When the differential input A is high, the bias current I_{SS} flows through the transistor MC2 and produces a low differential output voltage ($V_{OL} = V_Q - \overline{V_Q} = -I$). Conversely, when the differential input A is low, the bias current I_{SS} gets steered to transistor MC3 and produces a high differential output voltage ($V_{OH} = V_Q - \overline{V_Q} = I$). Thus, the voltage swing, V_{SWING} defined as the difference in the high and low output voltage is given as:

$$V_{SWING} = V_Q - \overline{V_Q} = 2I \quad (1)$$

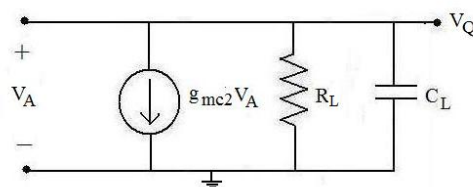
The voltage gain A can be computed by applying the half circuit concept [11]. The analysis of Fig. 1b gives A as:

$$A_{v_con} = \frac{V_Q(s)}{V_A(s)} = \frac{g_m}{1 + g_m R_L} \quad (2)$$

where R_L = load resistance, C_L is the load capacitance including the parasitic capacitances of the transistors in the PDN and the interconnect capacitances and g_m is the transconductance of the transistor MC2.



(a)



(b)

Fig.1. Conventional MCML inverter (a) circuit diagram (b) equivalent half circuit

III. SHUNT-PEAKED MCML STYLE

The shunt-peaking technique can be used to increase the speed of the conventional MCML circuits [8]. This technique uses an inductor (L) in series with a resistor () in the load such that the first-order RC circuit (2) is replaced with a second-order (RLC) circuit. Such circuits are named as shunt-peaked MCML circuits and may be abbreviated as MCML-SP circuits. A schematic of a MCML-SP inverter employing spiral inductor in the load is shown in Fig.2. When the differential input A is high, the bias current I_{SS} flows through the transistor MS2 and produces a low differential output voltage ($V_{OL} = V_Q - \bar{V}_Q = -I_s$) as the inductor L behaves as a short circuit to the constant inputs. Conversely, when the differential input A is low, the bias current I_{SS} is steered to the transistor MS3 and produces a high differential output voltage ($V_{OH} = V_Q - \bar{V}_Q = I_s$). Thus, for the equal values of and , the voltage swing, V_{SWING} of the MCML-SP circuits is same as that of the conventional MCML circuits.

The output impedance of the inverter, Z_i can be computed from Fig. 2b as:

$$Z_{out_sp} = \frac{R_{SP} + sL}{s^2 L C_L + s R_{SP} C_L}$$

(3)

which reduces to $Z_{out_sp} = R_{SP}$ when the input remain constant with the time (static case).

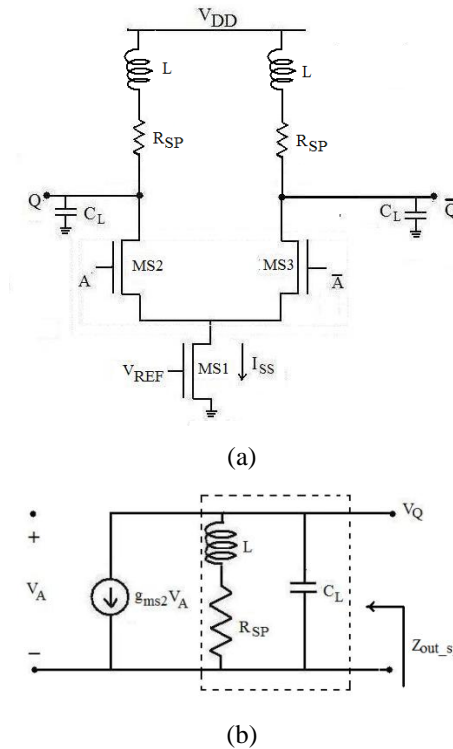


Fig.2. MCML-SP inverter with spiral inductor (a) circuit diagram b) equivalent half circuit

Using the half-circuit concept [11], the analysis of Fig. 2(b) gives voltage gain for the MCML-SP inverter

as:

$$A_{V_sp}(s) = \frac{V_Q(s)}{V_A(s)} = g_{ms2} Z_{out_sp} = \frac{g_{ms2}(R_{SP} + sL)}{s^2 L C_L + s R_{SP} C_L}$$

(4a)

where R_{SP} = load resistance, C_L is the load capacitance including the parasitic capacitances of the transistors in the PDN and the interconnect capacitances, L is the inductance and g_{ms2} is the transconductance of the transistor MS2.

In standard form [12], (4a) can be rewritten as:

$$A_{v_sp}(s) = \frac{(s+z)\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

(4b)

where ζ = damping factor = $\frac{R_{SP}}{2L\omega_n}$

(5a)

ω_n = natural frequency = $\frac{1}{\sqrt{LC}}$

(5b)

Depending on the value of the damping factor, ζ , the circuit can be overdamped ($\zeta > 1$), critically damped ($\zeta = 1$) and underdamped ($\zeta < 1$) and accordingly the time responses for the three cases differ. The presence of a LHP s-plane zero in Equation (4a) further tends to enhance the speed of the MCML-SP inverter in comparison to conventional MCML inverter.

IV. DESIGN OF MCML-SP CIRCUITS

In this section, an approach to size the transistors of the MCML-SP circuits for a given value of bias current, voltage gain and voltage swing is outlined. Then, the approach to design MCML-SP digital circuits is developed.

4.1 Design of MCML-SP inverter with spiral inductor load

The value of the load resistance R_{SP} (Fig. 2) can be evaluated by solving Equation (1) for the given values of the bias current I_{SS} and the voltage swing V_{SWING} as:

$$R_{SP} = \frac{V_S}{I_{SS}}$$

(6)

For a specific value of damping factor, ζ and a load capacitance C_L , the value of the spiral inductor can be computed from Equation (5a) as:

$$L = \frac{R_{SP}}{2\zeta\omega_n}$$

(7)

The voltage gain A_{v_sp} computed in (4a) is used to size transistors in the PDN. The aspect ratio of the transistors MS2 and MS3 can be calculated by using (4a) for the static case as

$$\left(\frac{W_N}{L_N}\right)_{MS2,3} = \frac{1}{\mu_{eff,n} C_{ox} I_{SS}} \left(\frac{A_n}{R}\right) \quad (8)$$

where C_{ox} is the oxide capacitance per unit area, $\mu_{eff,n}$ and R are the effective electron mobility, the effective channel width and length of the transistors MS2 and MS3 respectively.

4.2 MCML-SP digital circuit design

The design approach presented in section 4.1 for MCML-SP inverter design with spiral loads can be extended to design other MCML-SP circuits. The steps to design the load for the spiral inductor load remain same as explained in section 4.2. To design the PDN, firstly the size of the equivalent inverter is found out by using either Equation (8) depending upon the load and then individual transistors are sized according to the conventional approach for MCML circuits as discussed in [4].

V. SIMULATION RESULTS

This section first verifies the theoretical propositions presented in section 3 and 4. Thereafter, the performance of different logic gates based on MCML-SP style is compared with the conventional MCML style. The effect of parameter variations is also studied at different design corners. All the simulations are performed by using TSMC 0.18 μm CMOS technology parameters with a power supply of 1.8 V, bias current of 500 μA , voltage swing of 400 mV, and load capacitance of 400 fF.

5.1 Proposed MCML-SP Inverter

The methodology given in Section 3 and 4 is used to design spiral inductor load inverter with the outlined specifications for different damping factors. The simulations were performed to select the value of damping factor to achieve proper circuit operation and lowest propagation delay. The propagation delay for spiral inductor load inverter various values of damping factor, are listed in Tab. 1. It can be observed from the table that the propagation delay for the underdamped case is lower than the overdamped and the critically damped cases. For proper operation of the circuit, the overshoot should be less than 5% in the time response [12].

Keeping this in view, the case with $\zeta = 0.7$ gives the lowest propagation delay. Therefore, this value can be chosen as the optimum value to design MCML-SP circuits. Though, the inverter with spiral inductor outperforms. The sizes of the transistors for the spiral MCML inverter for $\zeta = 0.7$ are listed in Table 2. All the transistors have minimum channel length.

5.2 Performance Comparison

Several logic circuits such as AND/NAND, MUX, full adder, D-latch are designed with spiral inductor using the method outlined in section 4. The performance of these circuits is compared with their conventional

resistive and PMOS [4] load MCML counterparts. It may be noted that all the circuits operate at same supply voltage and bias current therefore they all consume same static power computed as the product of the supply voltage and bias current [4]. The propagation delay of the gate with respect to the above loads is listed in Table 3. It can be noted that a delay reduction varying from 21% to 29% is obtained by using inductive load.

The impact of parameter variation on the MCML-SP inverters and the conventional inverters is studied at different design corners. The findings for various operating conditions are given in Table 4. It is found that the propagation delay varies by a factor of 1.04, 1.15, 1.11 and 1.10 for the resistive, PMOS, spiral inductor load respectively between the best and the worst cases. It can be observed that they all show similar variations.

VI. CONCLUSION

The analysis and design of shunt-peaked MCML style for digital circuit design is presented in this paper. The logic style uses the shunt-peaking technique and suggests the use of inductors in the load. The design method is illustrated for shunt-peaked MCML inverter with the spiral inductors. The effectiveness of the shunt-peaked MCML style is demonstrated by simulating different logic gates. It is found that the shunt-peaked MCML circuits are faster than the other MCML variants. The study of impact of process variation at different design corners shows that conventional MCML and MCML-SP inverters show similar variations.

TABLE. 1. : Propagation delay of the MCML-SP inverter with spiral inductor load for various values of damping factor,

Damping factor,	Propagation delay with spiral inductor (ps)	Output response
2	120	Flat
1	107	
0.9	105	Overshoots (< 5%)
0.8	103	
0.7	98	
0.6	94	Overshoots (> 5%)
0.5	88	
0.4	75	
0.3	72	
0.2	71	
0.1	70	

TABLE. 2. Values of the components for the MCML-SP inverter for $\zeta = 0.7$

MCML-SP inverter with spiral inductor (Fig. 2a)	
Component	Value
MS1	W/L = 5.2 μm /0.18 μm
MS2, MS3	W/L = 17.5 μm /0.18 μm
R	0.4 K Ω
L	32 nH

TABLE. 3. Comparison in Propagation delay (ps) of MCML logic circuits using different type of loads

Circuit/Type of load		Resistor	PMOS	Spiral Inductor
Inverter				
AND/NAND		137	158	111
2:1 MUX		175	193	149
Full Adder	Sum	327	367	289
	Carry	332	381	290
D-Latch		195	225	161

TABLE. 4. Impact of parameter variations on propagation delay (ps) for different inverters

Topology	NMOS	T	F	S	F	S
	PMOS	T	F	S	S	F
Inverter with resistive load		127	125	130	129	128
Inverter with PMOS load		150	140	161	142	158
Inverter with spiral inductor load		100	95	106	105	104

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