Analysis and Design of MOS Current Mode Logic
Circuits with Active Inductor Load

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ABSTRACT
This paper presents the analysis and design of an improved version of conventional MOS current mode logic (MCML) known as the shunt-peaked MCML style (MCML-SP) is presented. This logic style employs inductors in the load. The analytical formulation of the shunt-peaked MCML inverter employing active inductor is derived. An approach to design shunt-peaked MCML inverter is also developed which is easily extended to realize complex shunt-peaked digital MCML circuits. The performance of the designed circuits is compared with their respective MCML counterparts through simulations using TSMC 0.18 µm CMOS technology parameters. A maximum delay reduction of 29 % is achieved for shunt-peaked MCML circuits. The impact of process variation on the MCML-SP and conventional MCML inverter at different design corners shows similar variations.

Keywords: Active Inductor, High-Speed, Digital Circuits, MCML, Shunt-Peaked

I INTRODUCTION
The tremendous advancements in the VLSI technology has led to the design of high-resolution mixed-signal applications. These applications demands high performance digital circuits to be fabricated with analog circuitry on the same silicon substrate. MOS current mode logic (MCML) style has been widely used to design of digital circuits for mixed-signal applications as they provide an analog friendly environment due to the low switching noise [1-6].

A high speed version of the conventional MCML logic style named as shunt-peaked MCML logic style has been suggested in literature [7, 8]. This logic style is based on the technique of shunt-peaking and involves the use of inductors. A variety of digital circuits based on the shunt-peaked MCML logic style has been suggested [8-10]. However, the detailed analysis and the design of the shunt-peaked MCML circuits are not presented in any of them. In this paper, the design of shunt-peaked MCML circuits through analytical modeling is put forward.
The paper first presents an overview of the conventional MCML style in section 2. Then, the analysis of the shunt-peaked MOS current mode logic style employing active inductors is presented in section 3. An approach to design shunt-peaked MCML inverter is formulated in section 4 which is extended for shunt-peaked digital circuits. A variety of digital circuits is designed and is compared with the conventional MCML counterparts through simulations using 0.18 µm TSMC CMOS technology parameters in section 5. The impact of process variation at different design corners is also studied. Finally section 6 concludes the paper.

II MOS CURRENT MODE LOGIC (MCML) STYLE

A conventional MCML circuit consists of three main parts: a pull-down network (PDN), a constant current source, and a load circuit. The PDN implements the logic function by applying the series-gating approach [4]. The constant current source MC1 provides the bias current $I_{SS}$ while the load resistor $R_L$ determines the voltage swing. A schematic of a conventional MCML inverter with differential input $A$ is shown in Fig.1. It works on the principle of current steering. When the differential input $A$ is high, the bias current $I_{SS}$ flows through the transistor MC2 and produces a low differential output voltage ($V_{OL} = V_Q - V_Q = -I_{SS}R_L$). Conversely, when the differential input $A$ is low, the bias current $I_{SS}$ gets steered to transistor MC3 and produces a high differential output voltage ($V_{OH} = V_Q - V_Q = I_{SS}R_L$). Thus, the voltage swing, $V_{SWING}$ defined as the difference in the high and low output voltage is given as:

$$V_{SWING} = V_Q - V_Q = 2I_{SS}R_L$$

(1)

The voltage gain $A_{v,con}$ can be computed by applying the half circuit concept [11]. The analysis of Fig. 1b gives $A_{v,con}$ as:

$$A_{v,con} = \frac{V_Q(s)}{V_A(s)} = \frac{g_{mc2}R_L}{1 + sR_LC_L}$$

(2)

where $R_L$ is the load resistance, $C_L$ is the load capacitance including the parasitic capacitances of the transistors in the PDN and the interconnect capacitances and $g_{mc2}$ is the transconductance of the transistor MC2.

![Diagram of a conventional MCML inverter](image-url)
III SHUNT-PEAKED MCML STYLE

The shunt-peaking technique can be used to increase the speed of the conventional MCML circuits [8]. This technique uses an inductor (L) in series with a resistor (RSP) in the load such that the first-order RC circuit (2) is replaced with a second-order (RLC) circuit. Such circuits are named as shunt-peaked MCML circuits and may be abbreviated as MCML-SP circuits. A schematic of a MCML-SP inverter employing spiral inductor in the load is shown in Fig.2. When the differential input A is high, the bias current $I_{SS}$ flows through the transistor MS2 and produces a low differential output voltage ($V_{OL} = V_Q - \bar{V}_Q = -I_{ss}R_{SP}$) as the inductor L behaves as a short circuit to the constant inputs. Conversely, when the differential input A is low, the bias current $I_{SS}$ is steered to the transistor MS3 and produces a high differential output voltage ($V_{OH} = V_Q - \bar{V}_Q = I_{ss}R_{SP}$). Thus, for the equal values of $R_{SP}$ and $R_L$, the voltage swing, $V_{SWING}$ of the MCML-SP circuits is same as that of the conventional MCML circuits.

The use of the spiral inductor has several restrictions such as large component size and lengthier design process. Therefore, an active inductor [8] can be used in place of spiral inductor as shown in Fig. 3. The schematic of a MCML-SP inverter employing the active inductor load along with its equivalent half circuit are shown in Fig. 4. The output impedance of the inverter, $Z_{out,ac}$ by neglecting substrate bias effect can be computed from Fig. 4b as:

$$Z_{out,ac} = \frac{s (C_{gs4} + C_{gd4}) + G_{BIAS}}{s^2 (C_{gd4} C_{gs4} + C_L C_{gs4} + C_L C_{gd4}) + s [G_{BIAS} (C_L + C_{gs4}) + g_{ma4} C_{gd4}] + \frac{1}{g_{ma4} G_{BIAS}}}$$

(3)

where $G_{BIAS} = 1/R_{BIAS}$ is the conductance in the active inductor, $C_L$ is the load capacitance including the parasitic capacitances of the transistors in the PDN and the interconnect capacitances, and $g_{ma4}, C_{gs4}, C_{gd4}$ respectively are the transconductance, gate-source capacitance and gate-drain capacitance of the transistor MA4. It can be observed that (7) reduces to $1/g_{ma4}$ for the static case.
The derivation of the voltage gain $A_{v_{ac}}$ for the MCML-SP inverter with active inductor load using in the half-circuit concept results in:
\[
A_{V,ac} = \frac{V_{Q}(s)}{V_{A}(s)} = g_{ma2}Z_{out,ac} = g_{ma2}\left[\frac{s}{s^2(C_{gd4}C_{gs4} + C_{L}C_{gs4} + C_{L}C_{gd4}) + G_{BIAS}(C_{L} + C_{gs4}) + g_{ma4}C_{gd4} + g_{ma4}G_{BIAS}}\right]
\]

(4a)

where \( g_{ma2} \) is the transconductance of the transistor MA2.

By assuming \( C_{gd4}C_{gs4} \ll C_{L}(C_{gd4}+C_{gs4}) \), the (4a) can be simplified as:

\[
A_{V,ac} = g_{ma2}\left[\frac{s}{s^2(C_{L}(C_{gd4}+C_{gd4})+G_{BIAS})}[G_{BIAS}(C_{L}+C_{gs4})+g_{ma4}C_{gd4}+g_{ma4}G_{BIAS}}\right]
\]

(4b)

In standard form [12], (4b) can be rewritten as:

\[
A_{V,sp}(s) = \frac{(s+2\omega_n^2)/s}{s^2+2\omega_n s+\omega_n^2}
\]

(4c)

Comparing (8b) with (8c), the value of the damping factor and natural frequency can be computed as:

\[ \zeta = \frac{1}{2} (C_{L} + C_{gs4} + \frac{g_{ma4}G_{BIAS}}{G_{BIAS}} C_{gd4}) \sqrt{\frac{G_{BIAS}}{(C_{gs4}+C_{gd4})C_{L}g_{ma4}}} \]  

(5a)

For large values of \( C_{L} \), (9a) can be approximated as:

\[ \zeta = \frac{1}{2} \sqrt{\frac{C_{L} G_{BIAS}}{(C_{gs4}+C_{gd4})g_{ma4}}} \]  

(5b)

natural frequency, \( \omega_n = \sqrt{\frac{g_{ma4}G_{BIAS}}{(C_{gs4}+C_{gd4})C_{L}}} \)  

(5c)

Depending on the value of the damping factor, \( \zeta \), the circuit can be overdamped (\( \zeta > 1 \)), critically damped (\( \zeta = 1 \)) and underdamped (\( \zeta < 1 \)) and accordingly the time responses for the three cases differ. The presence of a LHP s-plane zero in (4a) further tends to enhance the speed of the MCML-SP inverter in comparison to conventional MCML inverter.

**IV DESIGN OF MCML-SP CIRCUITS**

In this section, an approach to size the transistors of the MCML-SP circuits for a given value of bias current, voltage gain and voltage swing is outlined. Firstly, the design method for MCML-SP inverter with active inductor load is discussed. Then, the approach to design MCML-SP digital circuits is developed.
4.1 Design of MCML-SP inverter with active inductor load

For the active inductor MCML-SP inverter (Fig. 4), the output impedance derived in (3) reduces to \( \frac{1}{g_{ma4}} \) for the static case. By solving (1) and then equating to the impedance in the static case, the value of aspect ratio of the load transistors MA4 and MA5 for the given values of the bias current \( I_{SS} \) and the voltage swing \( V_{SWING} \) can be calculated as

\[
\left( \frac{W_N}{L_N} \right)_{MA4,5} = \frac{2I_{SS}}{V_{SWING} \mu_{eff,a} C_{ox} (V_{DD} - V_{T,n})}
\]  

(6)

where the parameters \( \mu_{eff,a} \), \( V_{T,n} \), \( W_N \) and \( L_N \) are the effective electron mobility, the threshold voltage, the effective channel width and effective channel length of the load transistors MA4 and MA5 respectively.

After determining the size of MA4 and MA5, the different capacitance values are computed. The gate-source capacitance \( C_{gs} \) is equal to the overlap capacitance between the gate and the source [4]. The gate-drain capacitance \( C_{gd} \) is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [4].

For a specific value of damping factor, \( \varsigma \) and load capacitance \( C_L \), the value of the \( G_{BIAS} \) can be computed by using (5b) as:

\[
G_{BIAS} = 4 \varsigma^2 \left( \frac{C_{gs,4} + C_{gd,4}}{C_L} \right) g_{ma4}
\]  

(7)

The aspect ratio of the transistors MA2 and MA3 in the PDN can be calculated by solving(3) for the static case.

\[
\left( \frac{W_N}{L_N} \right)_{MA2,3} = A_{V_{ac}} \left( \frac{W_N}{L_N} \right)_{MA4,5}
\]  

(8)

4.2 MCML-SP digital circuit design

The design approach presented in section 4.2 for MCML-SP inverter design with active inductor loads can be extended to design other MCML-SP circuits. The steps to design the load for the active inductor load remain same as explained in section 4.2. To design the PDN, firstly the size of the equivalent inverter is found out by using either (12) or (15) depending upon the load and then individual transistors are sized according to the conventional approach for MCML circuits as discussed in [4].

V SIMULATION RESULTS

This section first verifies the theoretical propositions presented in section 3 and 4. Thereafter, the performance of different logic gates based on MCML-SP style is compared with the conventional MCML style. The effect of parameter variations is also studied at different design corners. All the simulations are
performed by using TSMC 0.18 µm CMOS technology parameters with a power supply of 1.8 V, bias
current of 500 µA, voltage swing of 400 mV, and load capacitance of 400 fF.

5.1 Proposed MCML-SP Inverter

The methodology given in Section 3 and 4 is used to design active inductor load inverter with the
outlined specifications for different damping factors. The simulations were performed to select the value of
damping factor to achieve proper circuit operation and lowest propagation delay. The propagation delay for
active inductor load inverter various values of damping factor, are listed in Tab. 1. It can be observed from
the table that the propagation delay for the underdamped case is lower than the overdamped and the critically
damped cases. For proper operation of the circuit, the overshoot should be less than 5% in the time response
[12]. Keeping this in view, the case with $\zeta = 0.7$ gives the lowest propagation delay. Therefore, this value
can be chosen as the optimum value to design MCML-SP circuits. The sizes of the transistors for the active
inverter for $\zeta = 0.7$ are listed in Tab. 2. All the transistors have minimum channel length.

5.2 Performance Comparison

Several logic circuits such as AND/NAND, MUX, full adder, D-latch are designed with active inductor
using the method outlined in section 4. The performance of these circuits is compared with their conventional
resistive and PMOS [4], spiral inductor load MCML counterparts. It may be noted that all the circuits
operate at same supply voltage and bias current therefore they all consume same static power computed as
the product of the supply voltage and bias current [4]. The propagation delay of the gate with respect to the
above loads is listed in Tab. 3. It can be noted that a delay reduction varying from 21% to 29% is obtained
by using inductive load.

The impact of parameter variation on the MCML-SP inverters and the conventional inverters is studied
at different design corners. The findings for various operating conditions are given in Tab. 4. It is found that
the propagation delay varies by a factor of 1.04, 1.15, 1.11 and 1.10 for the resistive, PMOS, spiral inductor
and active inductor load respectively between the best and the worst cases. It can be observed that they all
show similar variations.

<table>
<thead>
<tr>
<th>Damping factor, $\zeta$</th>
<th>Propagation delay with active inductor (ps)</th>
<th>Output response</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>120</td>
<td>Flat</td>
</tr>
<tr>
<td>1</td>
<td>111</td>
<td>Overshoots (&lt; 5%)</td>
</tr>
<tr>
<td>0.9</td>
<td>108</td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>0.7</td>
<td>102</td>
<td></td>
</tr>
<tr>
<td>0.6</td>
<td>99</td>
<td>Overshoots (&gt; 5%)</td>
</tr>
<tr>
<td>-----</td>
<td>----</td>
<td>------------------</td>
</tr>
<tr>
<td>0.5</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td>0.4</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>0.3</td>
<td>88</td>
<td></td>
</tr>
<tr>
<td>0.2</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td>0.1</td>
<td>84</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Values of the components for the MCML-SP inverter for $\varsigma = 0.7$

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA1</td>
<td>$W/L = 5.2 \mu m/0.18 \mu m$</td>
</tr>
<tr>
<td>MA2, MA3</td>
<td>$W/L = 17.5 \mu m/0.18 \mu m$</td>
</tr>
<tr>
<td>MA4, MA5</td>
<td>$W/L = 8.65 \mu m/0.18 \mu m$</td>
</tr>
<tr>
<td>$R_{\text{BIAS}}$</td>
<td>7.34 KΩ</td>
</tr>
</tbody>
</table>

Table 3. Comparison in Propagation delay (ps) of MCML logic circuits using different type of loads

<table>
<thead>
<tr>
<th>Circuit/Type of load</th>
<th>Resistor</th>
<th>PMOS</th>
<th>Spiral Inductor</th>
<th>Active Inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AND/NAND</td>
<td>137</td>
<td>158</td>
<td>111</td>
<td>125</td>
</tr>
<tr>
<td>2:1 MUX</td>
<td>175</td>
<td>193</td>
<td>149</td>
<td>159</td>
</tr>
<tr>
<td>Full Adder</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sum</td>
<td>327</td>
<td>367</td>
<td>289</td>
<td>301</td>
</tr>
<tr>
<td>Carry</td>
<td>332</td>
<td>381</td>
<td>290</td>
<td>322</td>
</tr>
<tr>
<td>D-Latch</td>
<td>195</td>
<td>225</td>
<td>161</td>
<td>171</td>
</tr>
</tbody>
</table>

Table 4. Impact of parameter variations on propagation delay (ps) for different inverters

<table>
<thead>
<tr>
<th>NMOS</th>
<th>T</th>
<th>F</th>
<th>S</th>
<th>F</th>
<th>S</th>
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<tbody>
<tr>
<td>Topology</td>
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</tr>
<tr>
<td>NMOS</td>
<td>T</td>
<td>F</td>
<td>S</td>
<td>F</td>
<td>S</td>
</tr>
<tr>
<td>PMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inverter with resistive load</td>
<td>127</td>
<td>125</td>
<td>130</td>
<td>129</td>
<td>128</td>
</tr>
<tr>
<td>Inverter with PMOS load</td>
<td>150</td>
<td>140</td>
<td>161</td>
<td>142</td>
<td>158</td>
</tr>
<tr>
<td>Inverter with spiral inductor load</td>
<td>100</td>
<td>95</td>
<td>106</td>
<td>105</td>
<td>104</td>
</tr>
<tr>
<td>Inverter with active inductor load</td>
<td>115</td>
<td>108</td>
<td>119</td>
<td>117</td>
<td>118</td>
</tr>
</tbody>
</table>
6 CONCLUSION

The analysis and design of shunt-peaked MCML style for digital circuit design is presented in this paper. The logic style uses the shunt-peaking technique and suggests the use of inductors in the load. The design method is illustrated for shunt-peaked MCML inverter with the spiral and active inductors. The effectiveness of the shunt-peaked MCML style is demonstrated by simulating different logic gates. It is found that the shunt-peaked MCML circuits are faster than the other MCML variants. The study of impact of process variation at different design corners shows that conventional MCML and MCML-SP inverters show similar variations.

REFERENCES


