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Low Power and Low Area Analysis of real Time Validation and Verification SRAM Controller and 6T SRAM

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ABSTRACT

Any digital system requires memory to store the data and a controller to operate it. Generally hardware is used for computation with the memory. But these computations are permanently frozen by manufacturing process. So this kind of system can't provide flexibility to change the design. The proposed model is an integrated memory controller with its SRAM; which can be used for any real-time application.

Keywords:Front End Design, Back End Design, Static RAM or SRAM, 6T SRAM.

I.INTRODUCTION

A Memory controller and SRAM of size (256×8) are designed with VHDL coding. It is a prototype model using Xilinx" s Spartan FPGA.FPGA gives nearly all benefits of software flexibility and development model. This FPGA- based system can be reprogrammed many times or even new task can be performed. In the similar design aspect, we will consider the function parameters checks and validation/testing procedures for SRAM in regards to front End and Back end design.

One such case with back end, SRAM is designed to provide an interface with CPU and to replace DRAMs in systems that require very low power consumption. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/Nano ranges.

The scaling of CMOS technology has significant impacts on SRAM cell – random fluctuation of electrical characteristics and substantial leakage current. The random fluctuation of electrical property causes the SRAM cell to have huge mismatch in transistor threshold voltage. Consequently, the static noise margin (Read Margin) and the write margin are degraded dramatically. The SRAM cell tends to be unstable and the low power supply operation becomes hard to achieve. A 6T SRAM cell at 45 nm feature size in CMOS is proposed to accomplish low power memory operation. Initially, this paper presents design of 6T SRAM cell considering low power

consumption. The paper presents the design of SRAM array involving the decoders, sense amplifiers, transmission gates using Cadence tools

II. STATIC RANDOM-ACCESS MEMORY (STATIC RAM OR SRAM)

Static random-access memory is a type of semiconductor memory that uses bi-stable latching circuitry (flip-flop) to store each bit. SRAM exhibits data eminence, but it is still *volatile* in the conventional sense that data is eventually lost when the memory is not powered.

The term *static* differentiates SRAM from DRAM (*dynamic* random-access memory) which must be periodically refreshed. SRAM is faster and more expensive than DRAM; it is typically used for CPU cache while DRAM is used for a computer's main memory.

A. Clock rate and power

The power consumption of SRAM varies widely depending on how frequently it is accessed; in some instances, it can use as much power as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle – in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory structures.

B. SRAM exists primarily as:

- asynchronous interface, such as the ubiquitous 28-pin 8K × 8 and 32K × 8 chips (often but not always named something along the lines of 6264 and 62C256 respectively), as well as similar products up to 16 Mbit per chip with synchronous interface,
- usually used for caches and other applications requiring burst transfers, up to 18 Mbit (256K × 72) per chip integrated on chip

C. Embedded use

- Many categories of industrial and scientific subsystems, automotive electronics, and similar, contain static RAM.
- Some amount (kilobytes or less) is also embedded in practically all modern appliances, toys, etc. that implement an electronic user interface.
- Several megabytes may be used in complex products such as digital cameras, cell phones, synthesizers, etc.

SRAM in its dual-ported form is sometimes used for real-time digital signal processing circuits.

D. In computers

SRAM is also used in personal computers, workstations, routers and peripheral equipment: CPU register files, internal CPU caches and external burst mode SRAM caches, disk buffers, router buffers, etc. LCD

screens and printers also normally employ static RAM to hold the image displayed (or to be printed). Static RAM was used for the main memory of some early personal computers such as the ZX80, TRS-80 Model 100 and Commodore VIC-20

III. 6T SRAM

6T SRAM cell each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

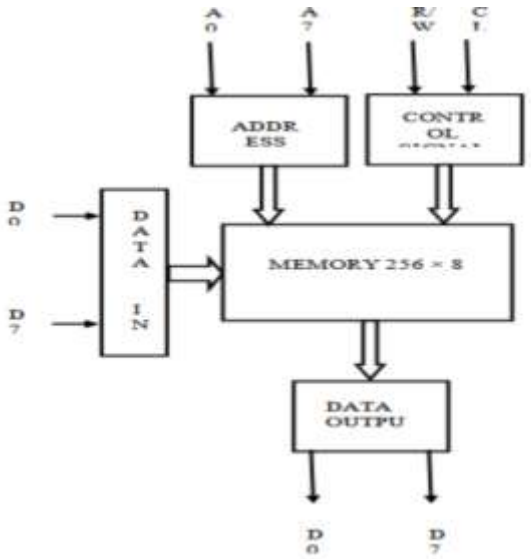
An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows: 2.1 STANDBY If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply. 2.2 READING Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second International Journal of Latest Trends in Engineering and Technology (IJLTET) Vol. 1 Issue 2 July 2012 45 ISSN: 2278-621X step occurs when the values stored in Q and Q bar are transferred to the bit lines by leaving BL at its recharged value and discharging BL bar through M1 and M5 to a logical 0. On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1. If the content of the memory were a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL-bar will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier is faster is the speed of read operation of SRAM. 2.3 WRITING the start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell i s needed to ensure proper operation. We can see from the figure that M5 and M6 transistor are connected to write line and M7 and M8 transistor are connected to read line and also these transistors are high voltage

transistor that means threshold voltage is higher for these transistors as compared to normal transistor. The difference between is more visible. The gate line is bold in case of high voltage NMOS transistor. In case of 9T SRAM, M7, M8, M9.

IV. FRONT END DESIGN

Design and Implementation of SRAM Controller using FSM for High Speed data transfer Applications

A. Structure of SRAM



The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations. Additional support circuitry used to implement special features, such as burst operation, may also be present on the chip. Figure shows a basic block diagram of a synchronous SRAM.

Figure shows the block diagram of memory (256×8). This has 8 bit address bus A0 to A7. The address inputs are used to select a memory location on the chip. When you select an address, you choose a memory location. For performance reasons, there are row and column address pins so that both may be selected at once. The number of address input pins depends on the size of the memory and how it is organized. For example, a 256 by 8 SRAM has 8 address input pins and 8 bit data bus from D0 to D7. This memory has got control signals R/W and Clock from controller.

B. System Block Diagram

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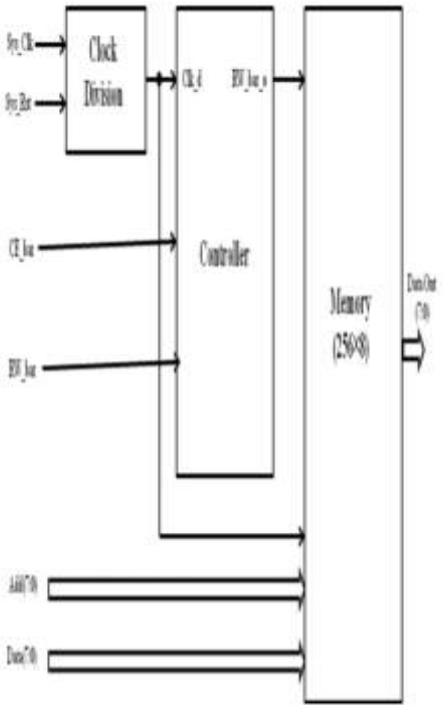
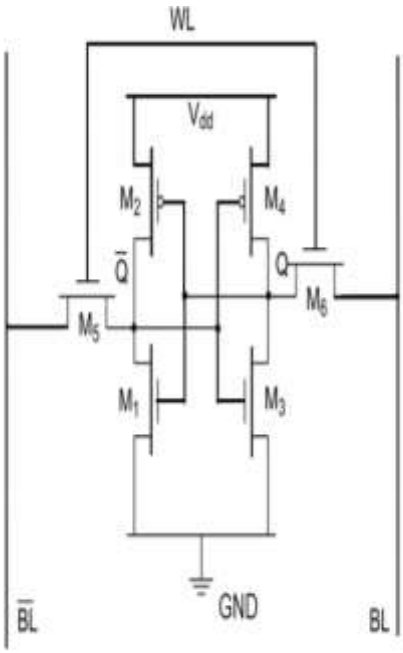


V. BACK END DESIGN

A. Design Block Diagram:



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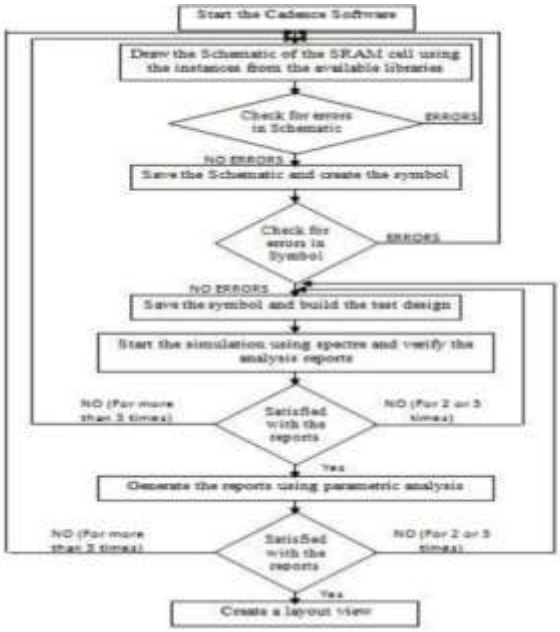
B. Design Flow for SRAM design



Software Tools Used:

Xilinx -Vivado2016

Model Sim Mentor Graphics

HDL designer Series Mentor Graphics, Cadence Virtuoso.

VI. CONCLUSION

Technology scaling demands a Low Power and Low Area Analysis of SRAM Controller and 6T SRAM In this paper, we present a Modified model using power reduction techniques that predicts the Low Area Analysis of SRAM Controller and 6T SRAM in real Time Validation and Verification, As the Proposed Model dissipates less power and has reduced delay it is useful for the design of memories in power efficient applications and less area occupation.

VII. ACKNOWLEDGEMENT

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