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Design and Implementation of DDRSDRAM controller and its architecture for Performance Improvement

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ABSTRACT

This project work is a working implementation of High Speed DDR (Double Data Rate) SDRAM Controller. The DDR Synchronous Dynamic RAM is an enhancement to the conventional SDRAM running at bus speed over 75MHz. The DDR SDRAM (referred to as DDR) doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal. The designed DDR Controller supports data width of 64 bits, Burst Length of 4 and CAS (Column Address Strobe) latency of 2.DDR Controller provides a synchronous command interface to the DDR SDRAM Memory along with several control signals. The DDR controller is designed with objective of proper commands for SDRAM initialization, read/write accesses, regular refresh operation, proper active and precharge command etc. DDR SDRAM controller is implemented using Verilog HDL and simulation and synthesis is done by using Modelsim and Xilinx ISE accordingly.

Keywords: Synchronous DRAM, Column Access Strobe, Row Access Strobe, Field Programmable Gate Arrays.

I.INTRODUCTION

Every computer system needs a memory area in which it can store the data on which it is working. This memory area is almost invariably made up of Random Access Memory (RAM). Random access memories can be both read and written. They are called random access because addresses can be read in any order. A RAM can be written an infinite number of times. The microprocessors can read data from the RAM quickly, faster than the ROM. The RAM forgets its data if the power is turned OFF. Hence the RAM is called the volatile memory. Usually RAMs are made up of cells consisting of MOSFETs. There is one cell each for a bit in the memory. Memory is made up of bits arranged in a two dimensional grid. In which memory cells are etched onto a silicon wafer in an array of columns (bit lines) and row (word lines). The intersection of a bit line and word line constitutes the address of the memory cell [2]. Two forms of RAM are Static RAM (SRAM) and Dynamic RAM (DRAM). A battery backed RAM is called Non Volatile RAM (NVRAM). Static RAM: The Static RAM uses a flip flop to store a bit of binary information or data. The static means that once a processor cycle writes a bit in a cell, it remains unchanged until it is modified in the processor cycle or until the power switches off.

There are four to six transistors per cell in a SRAM. An advantage of SRAM is that a write to it is static as long as the power is on and it does not require any refreshing circuit since it does not uses a capacitor in each cell. So static RAM is fast but is expensive. Dynamic RAM: Most bulk memory in modern systems is Dynamic RAM (DRAM). A DRAM uses tiny capacitor to store a bit of binary information. DRAM is very dense, but it requires that its values be refreshed periodically since the values inside the memory cells decay over time. An advantage of DRAM is that it stores a bit in less space than SRAM and is inexpensive. However it is slow since its memory locations need to be refreshed at regular intervals. Synchronous DRAM: The most dominant form of DRAM today, which uses clocks to improve the performance of DRAM, is Synchronous DRAM (SDRAM). Each cell is organized in rows and columns. SDRAM is arranged in banks of memory addressed by the row and column. The number of row and column address bits and number of bank defines the size of memory. SDRAM uses Row Address Select (RAS) and Column Address Select (CAS) signals to break the address into two parts, which selects the proper row and column in RAM array. Signal transitions are relative to the SDRAM clock that allows the internal operations of SDRAM to be pipelined. SDRAM uses a separate refresh control circuit to perform auto refresh operation. SDRAM has to be refreshed roughly once per millisecond. SDRAMs refresh part of the memory at a time instead of refreshing the entire memory at once. When a part of memory is being refreshed, it cannot be accessed until the refresh operation is completed. The memory refresh occurs over fairly few seconds so that each section is refreshed every few microseconds [6].

II.HISTORICAL REVIEW

Back in the 80s, PCs were equipped with RAM in quantities of 64 KB, 256 KB, 512 KB and finally 1 MB. Think of a home computer like Commodore 64. It had 64 KB RAM, and it worked fine.

Around 1990, advanced operating systems, like Windows, appeared on the market, that started the RAM race. The PC needed more and more RAM. That worked fine with the 386 processor, which could address larger amount of RAM. The first Windows operated PCs could address 2 MB RAM, but 4 MB soon became the standard.

The race has continued through the 90s, as RAM prices have dropped dramatically. Today no one is using less than 32 MB RAM in a PC. Many have much more. 128MB is in no way too much for a "power user" with Windows 95/98, it is important with plenty of RAM. SDRAM is widely used in computers, from the original SDRAM, further generations of DDR (orDDR1) and then DDR2 and DDR3 have entered the mass market, with DDR4 currently being designed and anticipated to be available in 2012.

Although the concept of synchronous DRAM has been known since at least the 1970s and was used with early Intel processors, it was only in 1993 that SDRAM began its path to universal acceptance in the electronics industry. In 1993, Samsung introduced its KM48SL2000 synchronous DRAM, and by 2000, SDRAM had replaced virtually all other types of DRAM in modern computers, because of its greater performance.

SDRAM latency is not inherently lower (faster) than asynchronous DRAM. Indeed, early SDRAM was somewhat slower than contemporaneous burst EDO DRAM due to the additional logic. The benefits of SDRAM's internal buffering come from its ability to interleave operations to

multiple banks of memory, thereby increasing effective bandwidth. Today, virtually all SDRAM is manufactured in compliance with standards established by JEDEC, an electronics industry association that adopts open standards to facilitate interoperability of electronic components. JEDEC formally adopted its first SDRAM standard in 1993and subsequently adopted other SDRAM standards, including those for DDR, DDR2 and DDR3SDRAM. SDRAM is also available in registered varieties, for systems that require greater scalability such as servers and workstations. As of 2007, 168-pin SDRAM DIMMs are not used in new PC systems, and 184-pin DDR memory has been mostly superseded. DDR2 SDRAM is the most common type used with new PCs, and DDR3 motherboards and memory are widely available, and less expensive than still-popular DDR2 products. Today, the world's largest manufacturers of SDRAM include: Samsung Electronics, MicronTechnology, and Hynix.

2.1 SDRAM (Synchronous Dynamic Random Access Memory):

"Synchronous" tells about the behaviour of the DRAM type. In late 1996, SDRAM began to appear in systems. Unlike previous technologies, SDRAM is designed to synchronize itself with the timing of the CPU. This enables the memory controller to know the exact clock cycle when the requested data will be ready, so the CPU no longer has to wait between memory accesses. For example, PC66 SDRAM runs at 66 MT/s, PC100 SDRAM runs at 100 MT/s, PC133 SDRAM runs at 133 MT/s, and so on.

SDRAM can stand for SDR SDRAM (Single Data Rate SDRAM), where the I/O, internal clock and bus clock are the same. For example, the I/O, internal clock and bus clock of PC133 are all 133 Mhz. Single Data Rate means that SDR SDRAM can only read/write one time in a clock cycle. SDRAM have to wait for the completion of the previous command to be able to do another read/write operation.

2.2 DDR SDRAM (Double Data Rate SDRAM):

The next generation of SDRAM is DDR, which achieves greater bandwidth than the preceding single data rate SDRAM by transferring data on the rising and falling edges of the clock signal (double pumped). Effectively, it doubles the transfer rate without increasing the frequency of the clock. The transfer rate of DDR SDRAM is the double of SDR SDRAM without changing the internal clock. DDR SDRAM, as the first generation of DDR memory, the prefetch buffer is 2bit, which is the double of SDR SDRAM. The transfer rate of DDR is between 266~400 MT/s. DDR266 and DDR400 are of this type.

2.3 DDR2 SDRAM:

Its primary benefit is the ability to operate the external data bus twice as fast as DDR SDRAM. This is achieved by improved bus signal. The prefetch buffer of DDR2 is 4 bit (double of DDR SDRAM). DDR2 memory is at the same internal clock speed (133~200MHz) as DDR, but the transfer rate of DDR2 can reach 533~800 MT/s with the improved I/O bus signal. DDR2 533 and DDR2 800 memory types are on the market.

2.4 DDR3 SDRAM:

DDR3 memory reduces 40% power consumption compared to current DDR2 modules, allowing for lower operating currents and voltages (1.5 V, compared to DDR2's 1.8 V or DDR's 2.5 V). The transfer rate of DDR3 is 800~1600 MT/s. DDR3's prefetch buffer width is 8 bit, whereas DDR2's is 4 bit, and DDR's is 2 bit. DDR3 also adds two functions, such as ASR (Automatic Self-Refresh) and SRT (Self-Refresh Temperature). They can make the memory control the refresh rate according to the temperature variation.

2.5 DDR4 SDRAM:

DDR4 SDRAM provides the lower operating voltage (1.2V) and higher transfer rate. The transfer rate of DDR4 is 2133~3200 MT/s. DDR4 adds four new Bank Groups technology. Each bank group has the feature of singlehanded operation. DDR4 can process 4 data within a clock cycle, so DDR4's efficiency is better than DDR3 obviously. DDR4 also adds some functions, such as DBI(Data Bus Inversion),CRC(Cyclic Redundancy Check) and CA parity. They can enhance DDR4 memory's signal integrity, and improve the stability of data transmission/access.

Table1: Comparison of DR/DDR2/DDr3/DDR3

DDR SDRAM Standard	Internal rate (MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.5
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2

III. DESIGN PHASE

The design part will be divided into two phases.

The Phase – I is basically the FRONT END DESIGN which comprises of:

1. Design of SRAM controller and SDRAM controller existing techniques.
2. Design of DDRAM controller with existing techniques.
3. Design Full-fledged architecture of SRAM,SDRAM and DDRAM using latest techniques.
4. Verification test bench procedure using system Verilog for all controller design.

The Phase – II is basically the BACK END DESIGN which comprises of:

1. Power Analysis of SRAM cell based design architecture for full read and write operations.
2. FPGA based Power reduction based on signalling.
3. SRAM cell reduction techniques and its implementations.

The basic functional block diagram of DDR SDRAM controller shown in fig.1 [3] consists of three modules:

i. The control interface module

ii. Command module or signal generation module and

iii. The data path module

1. Control interface module: The control interface module; is the primary module; consists of a finitestate machine shown in fig.2 and a programmable 16 bit counter to perform auto refresh operation. The controlinterface module accepts commands from the processor, decodes them and sends the decoded REFRESH, NOP,READA, WRITEA, PRECHARGE, and Load_MODE command to command module. The DDR SDRAM uses a separate clock: CLK and CLK` (the crossing of CLK going high and CLK` going low is considered as the positive edge of the clock). The commands are registered only on the positive edge of the clock. READ andWRITE are the basic commands used to access the SDRAM. The DDR SDRAM supports the burst length of 2,4, or 8 locations for programmable READ/WRITE operation. An access to the SDRAM starts at any assignedlocation and continues until the burst length is reached. The READ and WRITE operation start by sending theACTIVATE command.

2. Command module: The command module consists of an arbiter, multiplexer and three shift registers. An arbiter is used in case if multiple requests are arriving from different- different devices. If a high- priority and low- priority device both need to transmit data at the same time then the priority is given to high priority device. The low priority device will not be able to transmit data until the high priority device has sent all its data. In this work high priority is given to the REFRESH control operation. If the REFRESH operation is going on and the command from the host arrive then the controller will first continue the refresh operation and hold the command requests by not asserting the command acknowledge (CMDACK). Once the refresh operation is finished the command module will start performing the requested commands from the host. The shift registers are used to maintain the timing between the commands issued to the SDRAM. In addition to this the command module contains a multiplexer which is used to multiplex the address. The row address is multiplexed to SDRAM during the ACTIVATE (RAS) command. The column portion is multiplexed to SDRAM address outputs during a READ (WRITE) command [3].

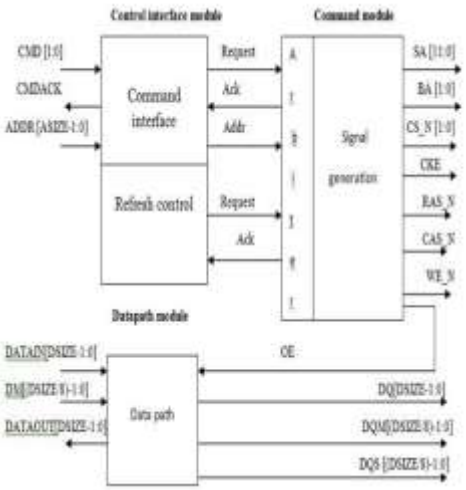

Fig 1 : Block Diagram of DDRSDRAM

3. Data path module: The data path module acts as an interface between the processor and the SDRAM. The data module only performs latching and dispatching of the data between the processor/host and the SDRAM. The data path module contains a tristate buffer which is controlled by the OE signal generated by the command module. The data to be written is received on the DATAIN pin during the WRITE operation and during the READA operation data is provided on the DATAOUT pin.

Softwares Used:

1. XILINX ISE
2. MODEL SIM
3. HDL DESIGNER SERIES

IV CONCLUSION

The design study shows that high-performance and large lookup table circuits can be implemented using low-cost state-of-the-art FPGA and DDR3 technology. The proposed DDR3 SDRAM Controller design has been verified by the exhaustive functional verification. We are trying to measure the performance of the design by generating several test cases and noting down the time taken by the designed DDR3 Controller in finishing them. In most of the scenario the throughput of the design will be close to the theoretical maximum.

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