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ANALYSIS OF LOW SUBTHRESHOLD SWING (SS) IN DOUBAL GATE JUNCTIONLESS TRANSISTOR

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ABSTRACT

In this paper, we analyzed the low sub-threshold swing (SS) in Double Gate Junctionless Transistor (n-type DG-JLT), which gives the combined advantages of both double gate junctionless FET and double gate tunnel FET. The DG-JLT is heavily n-type doped Si-channel JLT, where two isolated gates of different metal work-functions are used, the electrical behavior of DG-JLT resembles to conventional DG-FET structure.

Keywords—Double Gate Junctionless Transistor (DG-JLT), ION/IOFF ratio, low sub-threshold swing (ss).

1. INTRODUCTION

Dimensions of the MOSFET have continually been scaled down in size such that the effective channel length is approaching less than 22nm regime. The fabrication of steep doping profile for source and drain become critical. Careful fabrications of these junctions are necessary to achieve low thermal budget, low sub threshold slope etc. Very recently junctionless transistor has proposed and fabricated successfully by J.P colinge. which does not require any metallurgical junction, and is based on the Lilienfeld's first transistor architecture. As there is no requirement of ultra-sharp source and drain junctions for the JLT, the fabrication of this device would be simpler, have better electrical properties, and would be more robust compared to the conventional MOSFET.

A new field effect transistor structure, called double junctionless tunnel transistor (n-type DG-JLT,P-type DG-JLT),which gives the combined advantages of both double gate junctionless FET and double gate tunnel FET. The DG-JLT is heavily n-type or p-type doped Si-channel JLT, where two isolated gates of different metal work-functions are used; the electrical behaviour of DG-JLT resembles a conventional DG-FET structure. The primary principle applied here is to transform the equally doped n-type drain, channel and source regions of DG-JLT into a(N^+-I-P^+) structure for the DG-n JLT, and the equally doped p-type drain, channel and source of DG-JLT into a (P^+-I-N^+)structure for the DG-p JLT without any physical doping. Since this device is based on the principle of junctionless channel, intrinsically it would be less prone to variability and short channel effects(SCEs), as compared to the conventional FET, even with the requirement of an extra gate, and an isolation layer, and also an extra gate contact space, which increases few fabrications steps.

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II. DEVICE STRUCTURE

Junctionless transistor is turned off by complete depletion of the channel, using single gate it is difficult to fully deplete the channel. For better control on channel we require double gate structure. Fig. 1.1 show the schematic structure of double gate junctionless transistor (DGJLT). Device has same type of doping concentration for source, channel and drain. Common gate work function is used for both the gate.

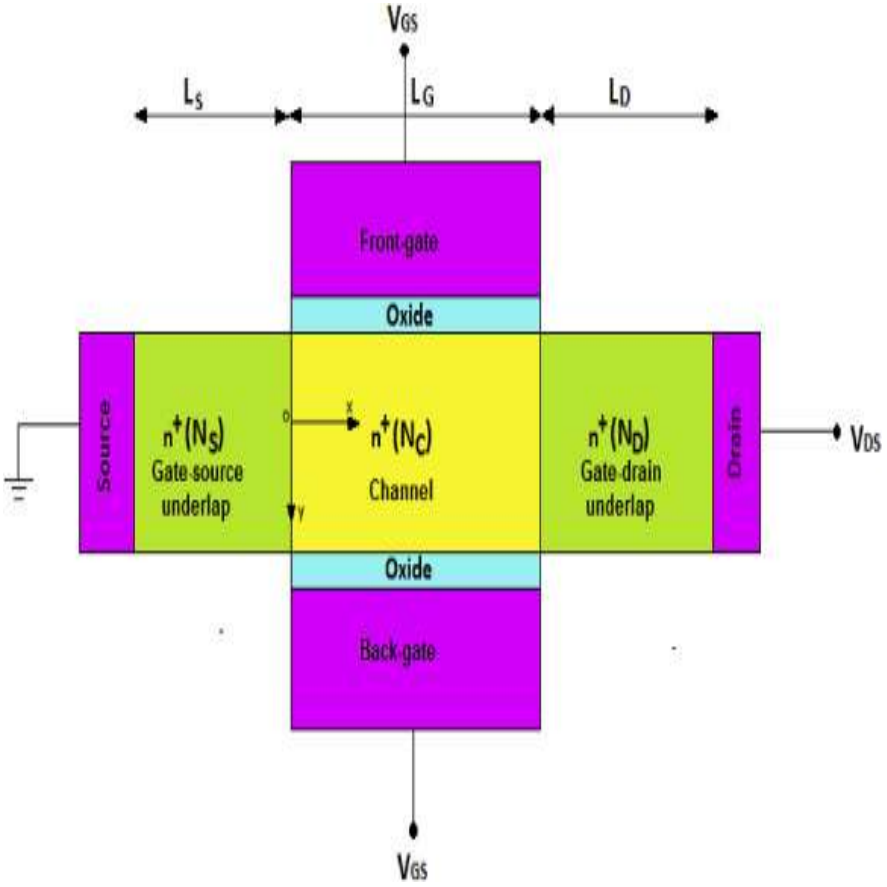

Figure 1.1 schematic structure of Double gate junctionless transistor

III.ENERGY BAND DIAGRAM OF DOUBLE GATE JUNCTIONLESS TRANSISTOR

Figure 1.2 shows energy-band diagrams of DGJLT in different operation of region in. off-state condition ($v_g<v_{th}$), channel is fully depleted, and immobile ions are present in channel. There is no conduction occurs in channel in this region (figure. 1.2(a)). For gate voltage greater than threshold voltage channel is moderately depleted and current conduction occurs through centre of the channel (Figure. 1.2(b)). Further increasing the gate voltage channel enters flat band region, channel is entirely neutral and since channels is highly doped semiconductor layer, so offers very high conductivity and current conduction occurs through entire device (Figure. 1.2(c)). For $V_g>V_{th}$, mobile carriers (electrons in N-channel device) start to accumulate in channel surface. Current conduction is mainly rule by mobile carriers and surface conduction occurs (Figure. 1.2(d)). In depletion and sub-depletion region current conduction is linear and current mainly flows through bulk of device and bulk conduction mechanism occurs.

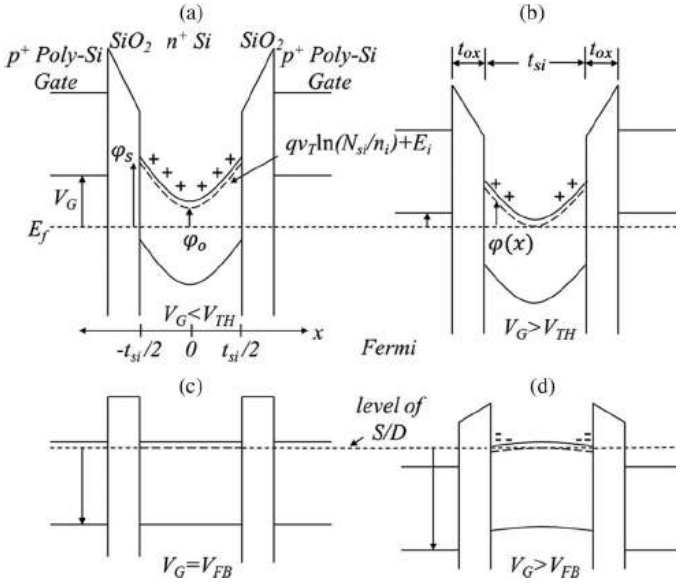

Figure 1.2 Schematic band diagram of the DGJLT. (a) Volume depleted and downwardly bent energy bands in the depletion region. (b) Moderate depleted and downward energy bands in the sub depletion region. (c) Flattened energy band in the flat band (d) Upwardly bend energy bands in the accumulation region[6]**.**

IV. EXPERIMENTAL RESULTS

The off-to-on switching capability of the MOSFET is represented by the slope of the drain current-gate voltage curve in sub-threshold operation, called the "sub-threshold slope". The sub-threshold slope of a classical transistor has a theoretical best value limit of 60 mV/decade at room temperature. That Value of sub-threshold slope is, unfortunately, no longer sufficient to ensure high on/off current ratios when supply voltages as low as 0.6 V are contemplated, and it becomes desirable to design transistors that have a sub-threshold slope lower than the theoretical limit of 60 mV/decade.

Impact ionization can be used in silicon-in-insulator (SOI) MOSFETs to obtain sub-threshold slopes below (kT/q)ln(10) = 60 mV/decade at room temperature. The mechanism for sub-threshold slope reduction involves impact ionization in the high-field region found at the drain junction when the device is in saturation. The hole current generated by impact ionization (we consider here an n-channel device) increases the potential of the transistor body in the channel region, which in turn decreases threshold voltage and increases the drain current. The increase of current increases the impact ionization rate, which completes a positive feedback loop. As a result of this positive feedback the device current latches rapidly from the off to the on state and sub-threshold slopes below 60 mV/decade can be observed. This effect was first described by Davis et al. in 1982 and has been widely documented since.

Table I lists different publications describing measurement of sub-threshold slope reduction using impact ionization. The Table lists the value of the sub-threshold slope _*SS*_ as well as the number of decades of drain current over which the effect is observed. To be complete, one needs to mention that "parasitic" bipolar junction

transistor action in the MOSFET's NPN structure can also be triggered, which accentuates the effect and creates hysteresis in the *ID*(*VG*)curves .It is generally accepted that the threshold energy for impact ionization is 1.5 times the energy band gap at room temperature which corresponds to 1.68 eV in the case of silicon but impact ionization currents have been detected in MOSFETs for drain voltages as low as 1.1 V. A heavily doped MOSFET without junctions, called the junctionless Multi-gate transistor, has recently been proposed.

SS (mV/dec)	V_{DS} (V)	Decades	Year	Measurement	Material	Ref.
130-73	3	4	1986	Experiment	Si	1
20	5	5	1990	Experiment+ simulation	Si	3
<5	1	1	2008		Si	4
<5	1	5	2008	Simulation	Ge	4
<10	11.6	2	2008	Experiment	Si	5

Table1.

The fabricated devices reported here have a width ranging from 20 to 50 nm, a thickness ranging from 5 to 10 nm and a gate length of 1 m. The gate oxide thickness is 10 nm and the buried oxide thickness is 340 nm. The junctionless transistors are n-channel devices with a uniform n-type doping concentration of 1019 cm−3 in the source, drain and channel region. Table1. Sub-threshold slope(*SS*), drain voltage (V_{DS}), number of decades over which SS<60 mV/decade, year of publication, type of measurement, and material used to fabricate SOI MOSFETs with impact-ionization reduction of the sub-threshold slope.

Figure 2.1 shows the measured drain current as a function of gate voltage in an inversion-mode pi-gate MOSFET. The device width is 40 nm and the channel length is 1 _m. When a drain voltage, *V*DS, of 3 V is applied, the sub-threshold slope, *SS*, is 63 mV/decade .*V*DS needs to be increased to 3.5 V or higher to obtain sub-60 mV/dec slopes. The curves are shown for both forward and reverse *VG* scans, and very little hysteresis is observed. Figure 2.2 shows the measured drain current as a function of gate voltage in a junctionless MOSFET. The device dimensions are the same as in Fig.2.2 In this device, sub-60 mV/dec

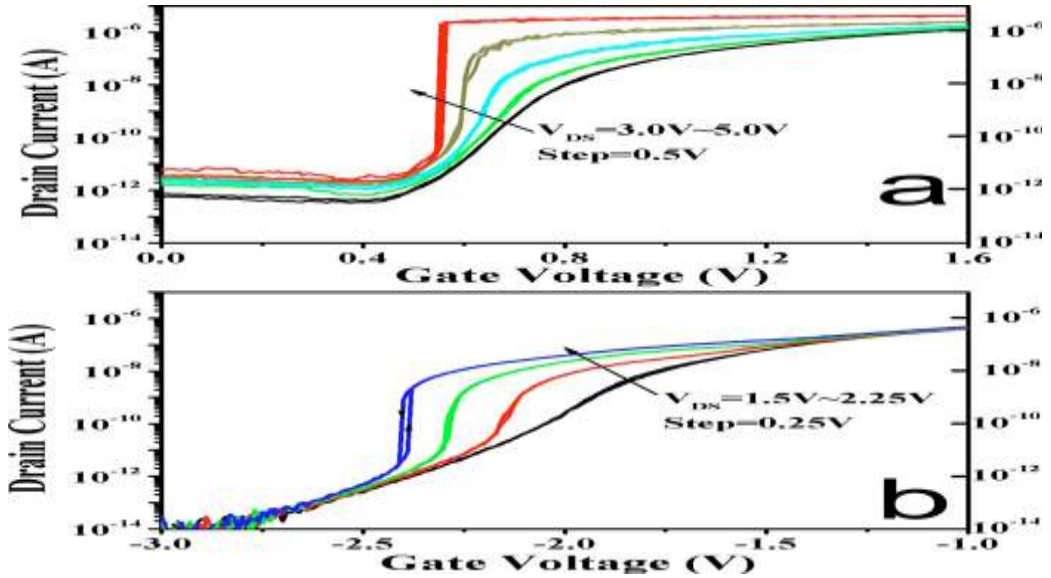

Figure. 2.1 (Color online) (a) Measured drain current vs gate voltage in an inversion-mode pi-gate nanowire MOSFET. *W*si=40 nm, *T*si=8 nm, *L*=1 µm; (b) Measured drain current vs gate voltage in a junctionless pi-gate nanowire MOSFET. *W*si=40 nm, *T*si=8 nm, *L*=1 µm.

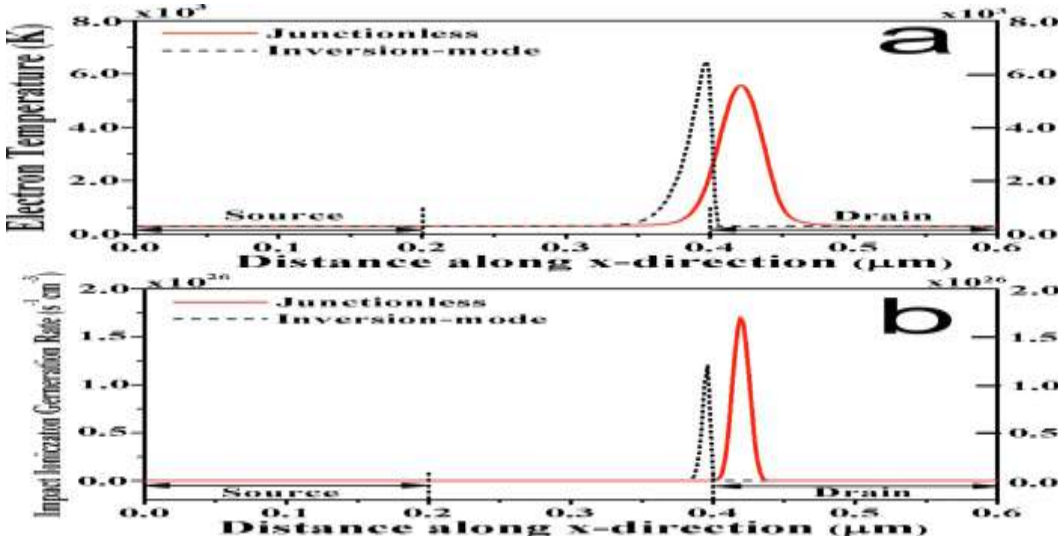

Figure. 2.2. (Color online) Simulated electron temperature (a) and Impact ionization rate (b) from source to drain in an inversion-mode pi-gate nanowire MOSFET and a junctionless pi-gate nanowire MOSFET. *V*DS=2.2 V, *V*GS=*V*TH−200 mV.

sub threshold slope appears for a drain voltage as low as 1.75 V, i.e., approximately half value needed for the standard inversion-mode device. A drain voltage of 1.75 V corresponds to 1.56 times the band gap energy of silicon. In order to understand why the effect of impact ionization is larger in the junctionless device, we have used numerical simulation tools. The devices were simulated using the ATLAS simulator9 using the following parameters for the junctionless devices: Silicon nano-wire width, *W*si=20 nm; silicon nano wire thickness, *T*si=5 nm, gate oxide thickness, *T*ox=10 nm, a gate length of 200 nm, and source/drain extension length of 200 nm.

The uniform n-type doping concentration in the nano wire is *ND*=1019 cm−3. Inversion mode pi-gate MOSFETs were simulated as well using the same parameters as the junctionless devices, but with p-type channel doping concentration of 2_1018 cm−3 in the channel region and n-type doping concentration of 1020 cm−3 in the source and drain.Figure2.2 shows the electron temperature and rate of impact ionization from the source contact (at x=0)to the drain contact (at x=0.6 µm). The part of the device covered by the gate electrode extends from x=0.2 to 0.4 µm. The drain voltage is 2.2 V and the gate voltage is set to be 200 mV lower than *V*TH, which is approximately the gate voltage at which corresponds the regions of minimum sub-threshold slopes are observed in Figure. 2.2 (a) and 2.2(b). The devices are turned off, and as expected, a high electric field is found at the drain junction of the inversion-mode pi-gate MOSFET, which holds the bulk of the applied drain bias. The peak field is in the channel region, right next to the metallurgical junction. In the junctionless device, the drain potential drop is found inside the drain electrode, outside of the region covered by the gate. This is because current blocking is caused by pure electrostatic pinch off of the heavily doped nano wire structure. The entire channel region is pinched off, and the bulk of the drain potential drop is found in the drain, near the gate electrode. Figure2.2 (a) shows

the electron temperature from source to drain in both devices. The impact ionization multiplication factor (M-1) is related to the electron temperature *Te* by the following relationship:

$(M-1)$ = integration of $\alpha Te(x)dx$;where α is the ionization rate.

V. CONCLUSIONS

In conclusion, double gated impact ionization is compared between standard inversion-mode multi-gate silicon transistors and

junctionless transistors. The region over which impact ionization takes place is found to be much larger in the junctionless devices, which reduces the drain voltage necessary to obtain a sharp sub-threshold slope. Based on these observations, one can speculate that using the junctionless MOSFET on germanium might make it possible to obtain sub-60 mV/dec slopes for drain voltages of 1 V or less. Higher on-state current and trans-conductance, lower drain induced barrier lowering sub-threshold slope and off-state current, increasing the *ION/IOFF* ratio.

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