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ANALYSIS AND SIMULATION OF MIXED CNTFET FOR VLSI INTERCONNECTS

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ABSTRACT

Latest developments in the field of VLSI Technology show an increasing interest in analog circuit design. The main aim of analog integrated circuits (ICs) is to satisfy circuit specifications through circuit architectures with the required performance. They can be used either as "stand-alone" topologies or connected to the digital part to implement mixed analog-digital functions, utilized in a wide field of applications.

Since the first CNTFET was reported in 1998, great progress has been made during the past years in all the areas of CNTFET science and technology, including materials, devices, and circuits. On the other hand, as the feature size of silicon semiconductor devices scales down to nanometer range, planar bulk CMOS design and fabrication encounter significant challenges. CNTFET among other new materials is promising due to the unique one-dimensional band-structure which reduces backscattering and makes near-ballistic operation. Exceptional electrical properties such as high speed, high-K compatibility, chemical stability, low SCEs have provided CNFETs with excellent characteristics which exceed those of the state of the art Si-based MOSFETs. Several researches have been done to estimate the performance of CNTFET at a single device level in the presence of process related non-idealities and imperfections at the 32 nm technology node using compact CNFET SPICE model. While seeking for solutions with higher integration, performance, stability, and lower power, carbon nanotube (CNT) has been presented for next-generation SRAM design as an alternative material in recent years. This study proposes a novel 7T SRAM cell based on CNTFET to reduce dynamic write-power and to improve the read cycle at the cost of minimal increase of cell area.

I.INTRODUCTION

Latest developments in the field of VLSI Technology show an increasing interest in analog circuit design. The main aim of analog integrated circuits (ICs) is to satisfy circuit specifications through circuit architectures with the required performance. They can be used either as "stand-alone" topologies or connected to the digital part to implement mixed analog-digital functions, utilized in a wide field of applications.

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It measures the application of one-dimensional fluid model in modeling of electron transport in carbon nanotubes and equivalent circuits for interconnections and compared the performances with the currently used copper interconnects in very-large-scale integration (VLSI) circuits. In this model, electron transport in carbon nanotubes is regarded as quasi one-dimensional fluid with strong electron-electron interaction. Verilog-AMS in Cadence/Spectre was used in simulation studies. Carbon nanotubes of the types single-walled, multiwalled and bundles were considered for ballistic transport region, local and global interconnections. Study of the S-parameters showed higher transmission efficiency and lower reflection losses. Theoretical modeling and computer-aided simulation studies through a complimentary CNT-FET inverter pair, interconnected through a wire, exhibited reduced delays and power dissipations for carbon nanotube interconnects in comparison to copper interconnects in 22 nm and lower technology nodes. The performance of CNT interconnects was shown to be further improved with increase in number of metallic carbon nanotubes. It measures the replacement of copper interconnect with the multiwalled and bundles of single-walled carbon nanotubes for the sub-nanometer CMOS technologies.

The study analyses the applicability of carbon nanotube (CNT) bundles as interconnects for VLSI circuits, while taking into account the practical limitations in this technology. A model is developed to calculate equivalent circuit parameters for a CNT-bundle interconnect based on interconnect geometry. Using this model, the performance of CNT-bundle interconnects (at local, intermediate and global levels) is compared to copper wires of the future. It is shown that CNT bundles can outperform copper for long intermediate and global interconnects, and can be engineered to compete with copper for local level interconnects.

II.STATEMENT OF THE PROBLEM

The main purpose of the study is to simulation of mixed CNTFET for VLSI interconnects and discuss the various issues related to it.

III.DELIMITATIONS

1. The study is delimited to the mixed CNTFET.
2. The study is also delimited to VLSI interconnects.

IV.LIMITATION

The facts discussed in this study will be based entirely on the responses to the algorithm and modeling of mixed CNTFET with VLSI interconnects, ascertaining the genuineness of the responses will identify as the limitation of the study.

V.PROPOSED SYSTEM

Carbon based electronic materials have been extensively studied in several of its allotropic forms such as carbon nanotubes (CNTs), atomic layers of graphite (i.e., graphene), fullerene molecules, and diamond for many years for applications such as resistive memories, logic devices, interconnect, biosensors, displays, solar panels, and many others. Moreover, it enables more aggressive design and enables more comprehensive testing.

VI.OBJECTIVES

- To study the carbon nanotube field-effect transistor.
- To examine the concept of CNTFET.
- To define the model of VLSI.
- To discuss the various algorithms related to it.
- To measure the various issues and challenges involved into it.

In the world of integrated circuits, CMOS has lost it's credential during scaling beyond 32nm. The main drawbacks of using CMOS transistors are high power consumption and high leakage current. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As technology is scaled down, the importance of leakage current and power analysis for VLSI design is increasing since short-channel effects cause an exponential increase in the leakage current and power dissipation. CNT-FET technologies mitigate these limitations by providing a stronger control over a thin silicon body. Enormous progress has been made to scale transistors to even smaller dimensions to obtain switching transistors that are fast and reduce the overall power consumption. However although the device characteristics are improved the problem of high active leakage still remain a problem. CNT-FET has become the most promising substitute to bulk CMOS technology because of reducing short channel effect and the similarity of the fabrication steps to the existing standard CMOS technology. CNT-FET device has a higher controllability, resulting relatively high on/ off ratio. CNT-FET devices can be used to increase the performance by reducing the leakage current and power dissipation. The research work has, characteristics of CNT-FET, inverter &basic gates like NAND Gate, and are modelled in HSPICE software using CMOS structures and CNT-FET structure are analysed and their performances like

power consumption and speed are compared. The values for Sub-Threshold slope of CNT-FET and MOSFETs are calculated.

Multi-walled carbon nanotubes (MWCNT) are promising candidates for futuristic Nano-electronic applications. MWCNT have potential to replace on - chip copper (Cu) interconnects due to their large conductivity and current carrying capabilities. Delay is one of the major design constraints in very large scale integration (VLSI) circuits. This paper presents an analysis of propagation delay and effect of repeater insertion on propagation delay for both MWCNT and Cu interconnects at different technology nodes viz 32nm and 22nm. In addition this paper deals with effect of voltage scaling in repeaters for long interconnects length in VLSI circuits in terms as propagation delay. It has been observed that propagation delay reduces with increase in bias voltage of the repeater at different interconnects length and technology nodes (32nm.22nm).

Majumdar et al (2013) Carbon nanotube (CNT) can be considered as an emerging interconnect material in current nanoscale regime. They are more promising than other interconnect materials such as Al or Cu because of their robustness to electromigration. This research paper aims to address the crosstalk-related issues (signal integrity) in interconnect lines. Different analytical models of single- (SWCNT), double- (DWCNT), and multiwalled CNTs (MWCNT) are studied to analyze the crosstalk delay at global interconnect lengths. A capacitively coupled three-line bus architecture employing CMOS driver is used for accurate estimation of crosstalk delay. Each line in bus architecture is represented with the equivalent RLC models of single and bundled SWCNT, DWCNT, and MWCNT interconnects. Crosstalk delay is observed at middle line (victim) when it switches in opposite direction with respect to the other two lines (aggressors). Using the data predicted by ITRS 2012, a comparative analysis on the basis of crosstalk delay is performed for bundled SWCNT/DWCNT and single MWCNT interconnects. It is observed that the overall crosstalk delay is improved by 40.92% and 21.37% for single MWCNT in comparison to bundled SWCNT and bundled DWCNT interconnects, respectively.

Channamallikarjuna Mattihalli et al (2012) attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Attempt to provide a multipurpose networking router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a self-independent VLSI Based router. The approach will results in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

M. Sowmya et al (2001) he attempt is to give a onetime networking solution by the means of merging the VLSI field with the networking field as now a days the router is the key player in networking domain so the focus remains on that itself to get a good control over the network. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need.

VII.SELECTION OF SUBJECTS

The performance of mixed CNT bundle interconnect is examined with carbon nanotube field effect transistor (CNFET) as a driver and compared with the VLSI interconnect, that is, CMOS driver on Cu interconnect. All HSPICE simulations are carried out at operating frequency of 1 GHz and it is found that mixed CNT bundle interconnects with CNFET as the driver can potentially provide a substantial delay reduction over traditional interconnects implemented at 32nm process technology. Similarly, the CNFET driver with mixed CNT bundle as interconnect is more energy efficient than the VLSI interconnect at all supply voltages (VDD) from 0.9V to 0.3 V.

VIII.RESEARCH METHODOLOGY

Research Methodology is a way to systematically solve the research problem, it not only takes the research methods but also consider the logic behind the methods. The study of Research Methodology for developing the project gives us the necessary training in gathering materials and arranging them, participation in the field work when required, and also provides training in techniques for the collection of data appropriate to particular problems.

IX.RESEARCH DESIGN

- Depth Interview: It refers that a specific type of qualitative marketing research method whereby data is received from a small group in hopes of determining the motivation for consumer purchasing decisions made.
- Secondary Data: Secondary data is the data that have been already collected by and readily available from other sources. Such data are cheaper and more quickly obtainable than the primary data and also may be available when primary data cannot be obtained at all.

X.DESCRIPTIVE STUDY

Cross-sectional Study: Cross-sectional research is a research method often used in developmental psychology, but also utilized in many other areas including social science and education. This type of study utilizes different groups of people who differ in the variable of interest, but share other characteristics such as socioeconomic status, educational background, and ethnicity.

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