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FINFET SRAM CELL USING INDEPENDENT GATE CONTROL

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ABSTRACT

CMOS devices are facing many problems because the gate starts losing control over the channel. These issues include improvement in leakage currents, increase of on current, increase in manufacturing cost, significant variations in parameters, less security, and yield, small channel results, etc. Considering typical CMOS is used to design SRAM, but it is also covering the difficulty of large power emission and increase in leakage current which changes its completion defective. Thoughts are expected to have short access time, less power dissipation and low leakage current thus FINFET based SRAM cells are recommended over CMOS based SRAM cells. Reducing the leakage aspects of the SRAM cells has been very essential to enhance the stability of the cell. Therefore many low power techniques are used to reduce the power dissipation and leakage currents. This project is about an independent-double-gate (IDG) fin-type MOSFET (FinFET) SRAM has been successfully fabricated with considerable leakage current reduction. The new SRAM consists of IDG-FinFETs which have flexible Fifth controllability. The IDG-FinFET with a TiN metal gate is manufactured by a newly developed gate-separation etching process. By appropriately controlling the Fifth of the IDG-FinFET, we have successfully demonstrated the reduction of the leakage current and power consumption of the SRAM circuitry.

Key Words*: *Dynamic Power dissipation, Energy Efficiency, FINFET, SRAM.

I. INTRODUCTION

The VLSI field, FINFET SRAM has been evolved as a revolutionary technology to offer 7nm size of transistor design to compensate for the need of superior storage system. The primary reason for this innovative technology is because of the three-dimensional model of the gate which lowers its controlling dependencies over current drain and source terminal. The conventional transistor device faces the problem of short channel effect, which denotes eliminated by present design principle of FINFET. Traditional MOSFET also suffers the question due to variations of arbitrary which is also removed due to FINFET as there is no channel doping mechanism in it. A catastrophic increase in static power consumption due to short channel effects (sce) is a severe problem in future VLSI circuits. In particular, the leakage current in the SRAM array is the most critical issue for low-power devices because it occupies a considerable part. The multigate MOSFET, particularly the fin-type MOSFET (finfet), is one of the most promising candidates for the scaled CMOS device owing to its high SCE

immunity.

Some finfet SRAM cells have moved studied for the scaled SRAM operation. However, the power consumption issue remains even for the finfet SRAM cell. Static RAMs are used widely in modern processors as on-chip memories due to their large storage density and small access latency. Static power is

the power dissipated in design in the absence of any switching activity. SRAM consumes more energy in VLSI systems, because of regular increase of on-die cache memory. One practical solution is to reduce leakage power and supply voltage to operate in the sub-threshold region. In the sub-threshold region, MOSFETs suffer from short-channel problems. That is due to weak channel control in these transistors in sub-threshold, which also leads to increased sensitivity to process variation in these devices. That sub-threshold leakage power is the main reason to increase the leakage power. This leakage is the only source of energy consumption in an idle circuit. Hence, the design of low-leakage SRAM cell is highly desirable. By the advancement of CMOS technology, SRAM undergoes considerable degradation of cell stability due to the variation in a Fifth of the cell. Accurate Fifth control is essential for high read stability. Similarly, variability and device leakage affect the writing ability of the cell. Read and write operation in SRAM is performed by using single bit-line of the battery, so both read stability and writeability problem are withdrawn. Partial selection takes place when word-line WL of the SRAM is ON, and the bit-lines are OFF leading to reduced security. In this paper, a new low-power internal write-back scheme is used to overcome the problem of partial selection during the write operation in SRAM. SRAM is a critical component in memory rich System on Chip (SoC) design. The conventional 6T SRAM cell has ample storage capacity but still suffers from sizeable dynamic power consumption, large leakage current and degraded read stability. Various subthreshold SRAM cells have been proposed to reduce the power consumption of the battery. Researchers have also introduced the new design technique to improve the security of the cell as well as to reduce the overall power consumption. Since now a day's SRAM cell is designed in the deep sub-micron region. Hence the extreme global and local variations and device mismatch cause the battery to lose its functionality.

In nano-scale CMOS memory, reducing minimum operation voltage, Vdd is becoming very difficult to do in conventional bulk CMOS. The limitation in low-voltage Vmin is one of the major problems. As the technology of device minimization is increased, various effects such as delay, voltage margin of circuit, increased dramatically in soft error rates, Vmin, etc. also increased,Vdd must be supplemented with device scaling to offset such effects, which causes an increase in the power dissipation, as well as degrades the device reliability due to increased stress voltage in any event, for the LSI industry in order to flourish and proliferate. Due to the variations in, various problems occur, such as delay or broader variations in circuit speed, degradation of voltage margins of flip-flops and increased soft-error rates (SER) in RAM cells and logic rates. Therefore, clarifying and solving the increasingly critical Vmin problem is extremely important in our future. The mainly describes the limitations that conventional MOSFET had and the solutions to low power the CMOS memories. These can be divided into three points of view. The first one is circuit design continue by material and finally is the new structure of MOSFETs. As power remains to be a significant concern in the battery-oriented and electronic devices, it is advisable to reduce it to some extent using CMOS technology. The considerable role of power consumption is observed in SRAM as it remains to be in idle mode for some time which in turn produces

leakage power in the devices. An increment in leakage power is examined with the scaling of device dimensions. Therefore, we reduce the supply voltage of SRAM.

II. CMOS BASED SRAM

An SRAM cell is the critical component storing a single bit of binary information. A 6T CMOS SRAM cell is viral in the IC industry due to its lowest static power dissipation among various circuit configurations. Also, the CMOS Cell offers superior noise margins. It has two cross-coupled inverters forming a latch and two n-type access transistors. The gate terminal of the access transistors is connected to the word line (wl), and a source terminal is connected to bit line (bl) and bit line bar (blb) individually. Whenever the concept element is to be used for reading or write operation, the access transistors must be switched ON. There is a requirement that SRAM cell should provide wider noise margin and high speed but it is a significant problem because if we require top rate when that leakage power increases [6]. A different difficulty with conventional planar SRAM is that primarily scaled technologies mean used in design principle of SRAM that provides smaller size with minimum supply voltage. The presents us with a little difference between the cut-off voltage and the supply voltage. Sometimes this close difference becomes highly unstable especially when the design requires increases in the number of transistors with the reduced size to maintain significant storage points [6]. Device design for an SRAM equals directed by the stability, power consumption, and access time of an SRAM cell.

III. LITERATURE REVIEW

The Scaling in Silicon technology, usage of SRAM Cells has been increased to the large extent while designing the embedded Cache and system-on-chips in CMOS technology. Power consumption, packing density and the speed are the significant factors of concern for developing a chip. The waste of power and speed of SRAMs are some critical issues among some elements that provide a solution which describes multiple designs that minimize the consumption of energy, and this review article implies also based on that. This report presents the simulation of 6T, 9T, LP10T, ST10T and WRE8T SRAM cells[1-10]. All the simulations have been carried out on 90nm at Micro wind EDA the seriousness of process variation in rooted sub-micron devices; it is necessary to study the operation of the rationed structure under process variations and device mismatch. The global and local changes can cause the traditional distributed logic to lose functionality[11-14].The Static Random Access Memory (SRAM) is highly rationed and affected by the global and local process fluctuations. In this paper, the proposed SRAM cell has been studied for the statistical process variations. The battery shows the improved read stability and writeability due to the isolation of reading and writes circuits. The cell shows robustness against temperature, process and voltage variation due to separate write signal WS, lower leakage current and smaller parasitic capacitance. The Low-power consumption in memory plays an integral part in VLSI[15-18]. Proposed 10T SRAM design is used to reduce the leakage power and to obtain better performance at minimum VDD compared with a conventional design. Another major problem suffered by SRAM during the write operation is Partial-selection of cells. Therefore, a new 10T SRAM is designed using unique low-power internal write-back scheme. To obtain low-voltage and low-leakage power 10T SRAM can be developed based on FinFET technology.

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IV .PROPOSED SYSTEM

The SRAM cell with p-MOS access transistors in which the BG of the access transistors means compared to the adjacent storage nodes. We call this structure as APBG structure. During a read operation, the β-ratio (β-ratio=WPL/WAPL) of the APBG cell means developed by the BG voltage of the APL.This increase in β-ratio improves the SNM during the reading operation. For example, in a 22-nm double gate FinFET technology with the same gate work function at 1 V, the read SNM of the APBG structure is improved by 1.83X compared to the DGP design. However, by decreasing each column. Hence their area and power overhead are negligible. We call our proposed cell as RAPBG (Robust SRAM with p-MOS access and built-in feedback). A robust FinFET SRAM design with p-MOS access transistors using independent gate (IG) control method. This model is performed by dynamically adjusting the back-gate (BG) voltages of pull-down (PD) electronics. For generating optimum PD, BG voltages, we use an extra write driver, pre-discharge circuit and n-MOS switches for write, hold and read operation respectively. Mixed mode TCAD simulations for the physical gate length of 22 nm, indicating that the proposed cell has the highest read SNM and Writeability, and the least static power dissipation than recently reported cells.

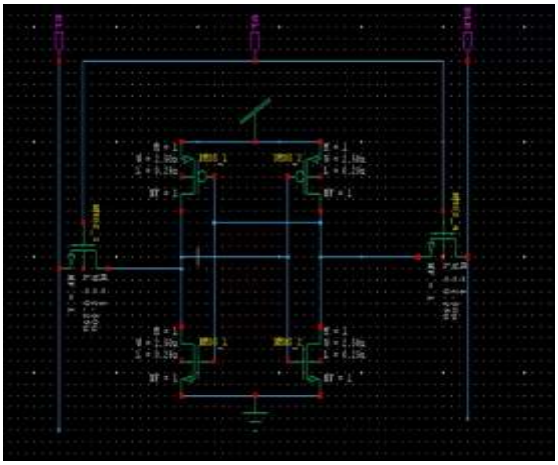
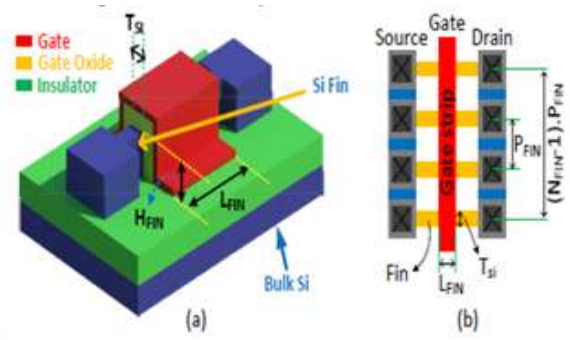


Figure.1 Proposed Circuit diagram

A FINFET TECHNOLOGY

The finfet device is a quasi-planar double-gate transistor. Compared with bulk CMOS this structure allows FinFET accessories to enhance the energy efficiency, ON/OFF current ratio, and soft-error immunity. The FinFET technology is immediately used as an alternative to the bulk CMOS for improved scalability. The three-terminal FinFET device structure where both gates remain shorted. Here HFIN is a height of the silicon fin, TSI is the thickness of the silicon fin, and LFIN is gate length of the spine. The layout of a three-terminal FinFET with four fins the main component is the fin which provides the channel for conducting current when the device is switched on. The gate is on either side of the vertical fin; it helps to reduce the leakage current and the short-channel effects. The ten transistor cell configuration is used to improve the stability of the cell and is used for subthreshold purposes.

The right internal value on the write-bit line means settled without going through the whole rewriting process to eliminate the state of half selection. So there will be no false changing of internal nodes in the design translating to lower power overhead compared with previous writeback schemes. The right internal value on the write-bit line implies settled without going through the whole rewriting process to eliminate the state of half selection. So there will be no false changing of internal nodes in the design translating to lower power overhead compared with previous writeback schemes.



FINFET Device: (A) Structure, (B) Layout

Figure 2: FINFET Device

V. SIMULATION RESULTS

The proposed system that is going to be defined in this phase is done using the tanner model. To get the desired output, the simulation circuit has been designed in tanner software by using the respective components that are present in the tanner.

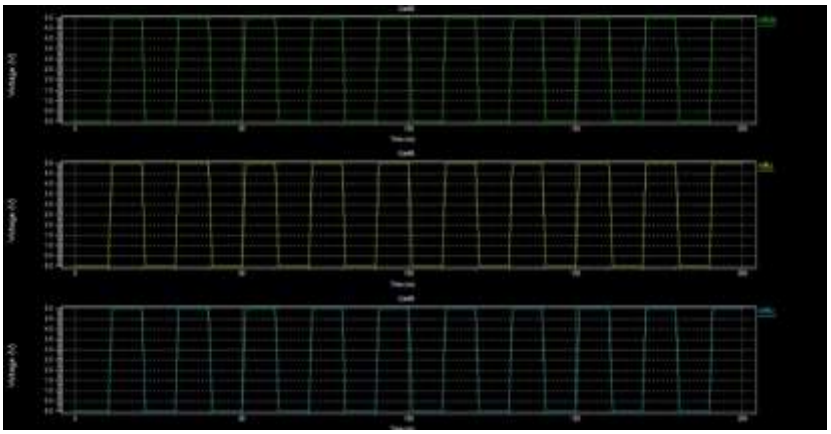


Figure 3: voltage current output waveform

TABLE I

An Efficient Timing Analysis Model For 6t Finfet Sram Using Current-Based Method

SRAM Operation	CSM Delay	Hospice Delay	Error Rate
Write	2.70ps	2.71ps	0.37%
64 Array Read	5.30ps	5.43ps	0.37%
128 Array Read	9.65ps	9.54ps	2.39%

256 Array Read	17.61ps	17.72ps	0.62%
512 Array Read	35.08ps	34.09ps	2.83%

TABLE II

Evaluation Of reading- And Write-Assist Circuits For Geoi Finfet 6t Sram Cells

FinFETs	GeOi/SOI
Lg(nm)	18
Wfin(nm)	7
Hfin(nm)	16
EOT(nm)	0
TBOX(nm)	10
Nch(CM-3)	1e16
NSD(CM-3)	5.5e19/1w20

VI. CONCLUSION

In this project, fabricating the IDG-FinFET SRAM with considerable leakage current reduction. We used advanced FinFET fabrication processes to integrate IDG-FinFETs for the proposed SRAM. We demonstrated the decline of not only the standby leakage current but also the dynamic power consumption by appropriately controlling the Fifth of the IDG-FinFET. Although the leakage current of low-Fifth IDG-FinFET is higher than that of the conventional CDG-FinFET, row-by-row Fifth control can allow the average leakage current of the IDG FinFET SRAM to be much lower than that of the CDG-FinFET SRAM. Thus, the fabricated IDG-FinFET SRAM is promising for the future scaled SRAM circuitry.

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