International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.(02), March 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

16 BIT APPROXIMATE MULTIPLIER USING MULTIPLEXER AND COMPRESSOR

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ABSTRACT

Approximate circuits can reduce the complexity of the design with better power efficiency and delay for the applications like multimedia signal processing and data mining applications.where exact outputs are not always necessary. The partial products of the multiplier are altered y using the generate and the propagate signals.For high speed application .compressor can be designed by using the mux,finally the multiplier simulated by using cadence with 45nm technology then the power and timing reports are obtained.

I.INTRODUCTION

Multiplication is the fundamental operation in most of the application.Generally multipliers have large area and delay. The design of the multiplier with low power can be a big challenges in the vlsi design.Generally the partial products are altered by using the adder circuits. In adders xor gate tend to more area and delay. So that mux can be used instead of adders to reduce the area.Truncation can be widely used to reduce the hardware complexity of the design.In truncation to reduce the quantization error constant term is added.The proposed multiplier uses mux for the reduction of partial products.The proposed compressors used in[2] produce high speed multiplication.the proposed high speed compressor reduce the number of gates.so that the area can be decreased. The proposed 8-4 compressor can be designed to reduce the partial products. There are 5 inputs in the 4-2 compressor and 4 outputs .one carry and 2 other outputs.In existing method [1] full adders and half adders are used to reduce the partial products.this multiplier designed in[1] require more adders to compute the result.

Uneven signal propagation of the adders increase the dynamic power consumption. In [3] approximate 4-2 compressor can be designed ,the main drawback of this design is they give non zero output even the inputs are zero. Which increase the error .

II.PROPOSED DESIGN

Implementation of multiplier consists of the following steps

1)partial product generation

2) Altered partial products using propagate and generatesignals

3)reduction of partial product

4)vector merge addition using parallel prefix adder

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A 16 bit unsigned number is used for illustration to describe the proposed method in approximation of multipliers.2 designs of approximate multipliers can be presented.

1)multiplier design using compressors

2)multiplier design using mux

Consider the two 16 bit un signed input operands

$$A=\sum_{m=0}^{15} a_m 2^m$$

$$\mathbf{B}=\sum_{m=0}^{15} b_m 2$$

The partial products $pp_{m,n}=a_m b_n$. The partial products are generated simply the AND operation between the bits of $a_m b_n$

III.GENERATION OF PARTIAL PRODUCTS

There are 62 partial products. The partial products are altered to produce the final output

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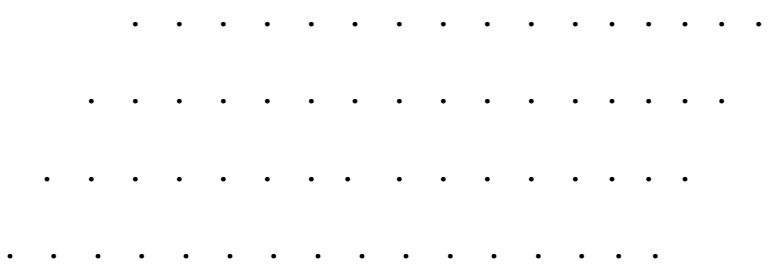


Fig1 : partial product generation

The column having more than 5 partial products are altered by using propagate and generate signals.

$$P_{m,n}=a_{m.n}+b_{n,m}$$

$$G_{m,n}= a_{m.n}*b_{n,m}$$

The number of generate signals increases the probability of error .To reduce the error the maximum number of generate signals to be grouped by or gate and it is kept at 4 . If the colun having m number of generate signal then (m/4) OR gates are used. In the proposed approximate multiplier 28 OR gates are used to group the generate signal

IV.ARCHITECTURE

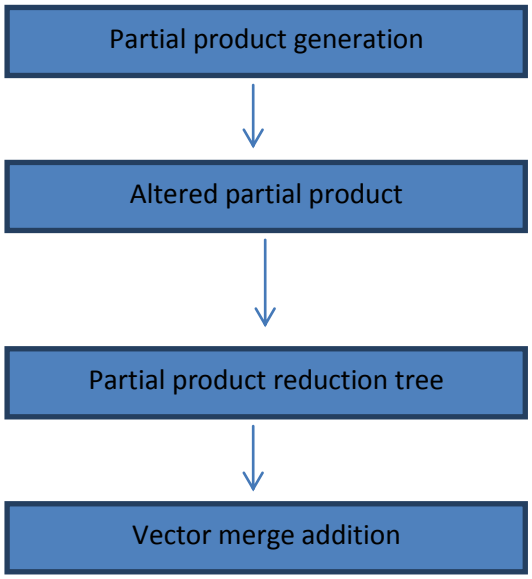


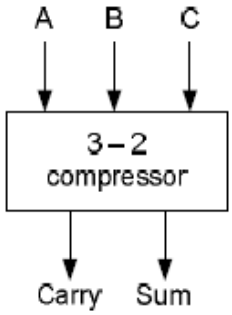
Fig2: proposed architecture

V.REDUCTION OF PARTIAL PRODUCTS

The partial products are further reduced by using multiplexers and compressors.The compressors are also designed by using the multiplexers. Multiplexers give fastest multiplication than adders also multiplexers require less amount of gates and produce less delay so that multiplexers are preferred than adders.

3-2 Compressor

In Figure 4 is presented the 3-2 adder compressor. As shown in the truth table, the operation is the same ofthe full adder. It takes 3 inputs A, B, C to generate 2 outputs, the sum and the carry bits.



A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig3(a):3-2 adder compressor. Fig (b):Truth table for the 3-2 adder compressor.

This compressor is governed by the following equation:

A+B+C=sum+2*carry

In Figure 3 are shown the two architectures implemented in this work. The traditional architecture is shown in Figure 3(a) and is implemented using the CMOS logic style of the XOR-XNOR and MUX modules. This architecture is governed by the following equations.

$$Sum = A \oplus B \oplus C$$

$$Carry = (A \oplus B) * C + \overline{(A \oplus B)} * A$$

4-2 Compressor

The 4-2 Compressor has 5 inputs A, B, C, D and Cin to generate 3 outputs Sum, Carry and Cout as shownin Figure 4(a). The 4 inputs A, B, C and D and the output Sum have the same weight. The input Cin is the output from a previous lower significant compressor and the Cout output is for the compressor in the next significant stage. The conventional approach to implement 4-2 compressors is with 2 full adders connected

serially as shown in Figure 4(b).

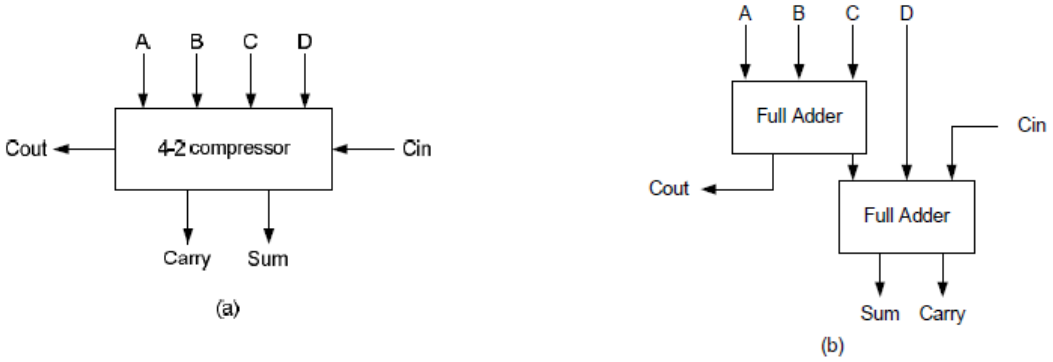


Fig 4:4-2 compressor

The 4-2 compressor is governed by the following equation:

$$A + B + C + D + Cin = SUM + 2 * (CARRY + Cout)$$

In Figure 7 are shown the two architectures implemented in this work. The traditional architecture is shown in Figure 7(a) and uses the CMOS logic style of the XOR-XNOR and MUX modules similarly to the 3-2 compressor. This architecture is governed by the following equations:

$$Sum = A \oplus B \oplus C \oplus D \oplus Cin$$

$$Cout = (A \oplus B) * C + \overline{(A \oplus B)} * A$$

$$Carry = (A \oplus B \oplus C \oplus D) * Cin + \overline{(A \oplus B \oplus C \oplus D)} * D$$

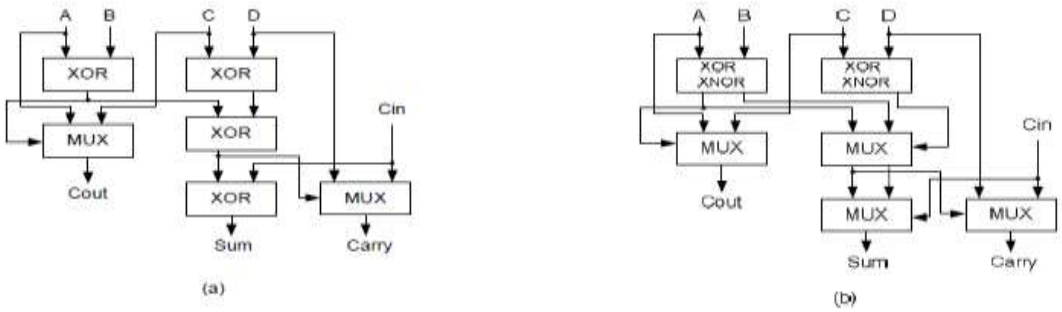


Fig. 5: (a) Traditional architecture of 4-2 Compressors. (b) Enhanced architecture with the XOR-XNOR and MUX modules of a 4-2 Compressor.

In Figure 5(b) is shown the enhanced version of the 4-2 compressor architecture. This architecture uses the XOR-XNOR module presented in Figure 3(a) and the transmission gate version of the MUX module presented in Figure 3(b). This architecture is governed by the following equations:

$$Sum = \left((A \oplus B) * \overline{(C \oplus D)} + \overline{(A \oplus B)} * (C \oplus D)\right) * \overline{Cin} + \left((A \oplus B) * \overline{(C \oplus D)} + \overline{(A \oplus B)} * (C \oplus D)\right) * Cin$$

$$Cout = (A \oplus B) * C + \overline{(A \oplus B)} * A$$

$$Carry = (A \oplus B \oplus C \oplus D) * Cin + \overline{(A \oplus B \oplus C \oplus D)} * D$$

Structure of 8-4 and 9-4 Compressors Using Multiplexer

The following figure shows the design of 8 to 4 compressor using mux

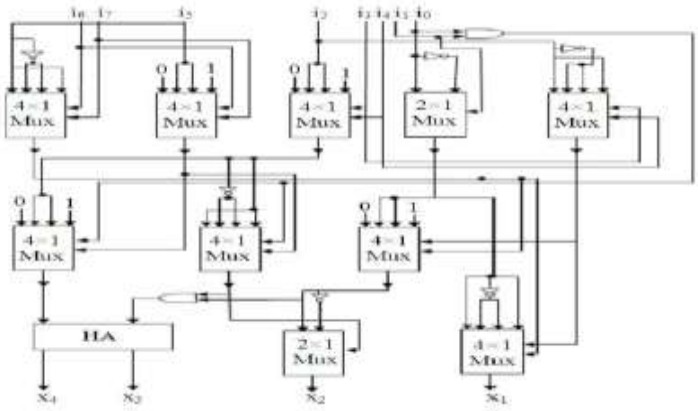


fig6(a):8-4 compressor

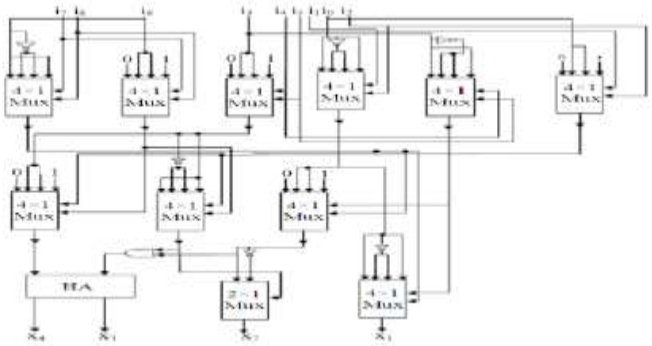


Fig 6(b):9-4 compressor

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VI.RESULT AND DISCUSSION

The following simulated output can be obtained by using the cadence software.The power and area can be reduced .In the finalstage of vector merge addition the parallel prefix adder can be used for the accumulation of partial products. Finally the parallel prefix adder produce the output as product. Here 32 bit parallel prefix adder can be used.

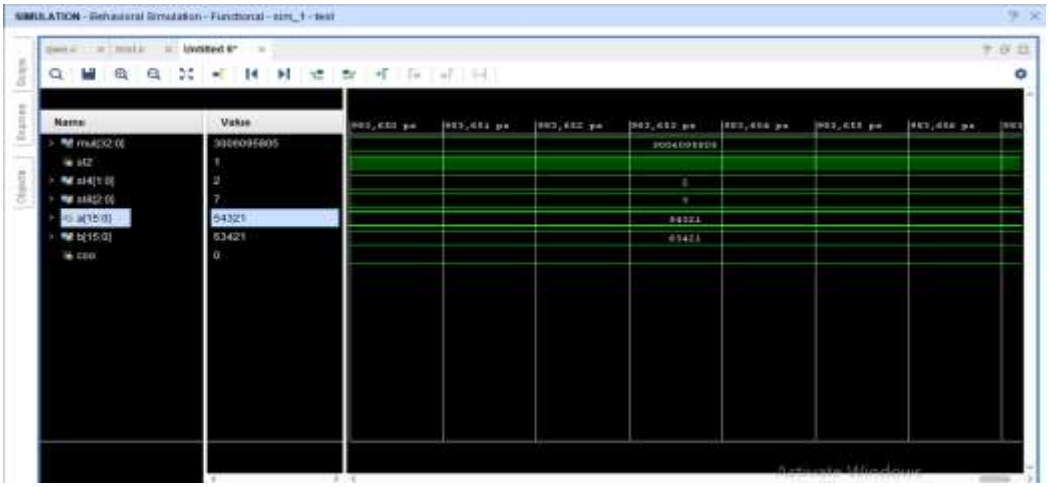
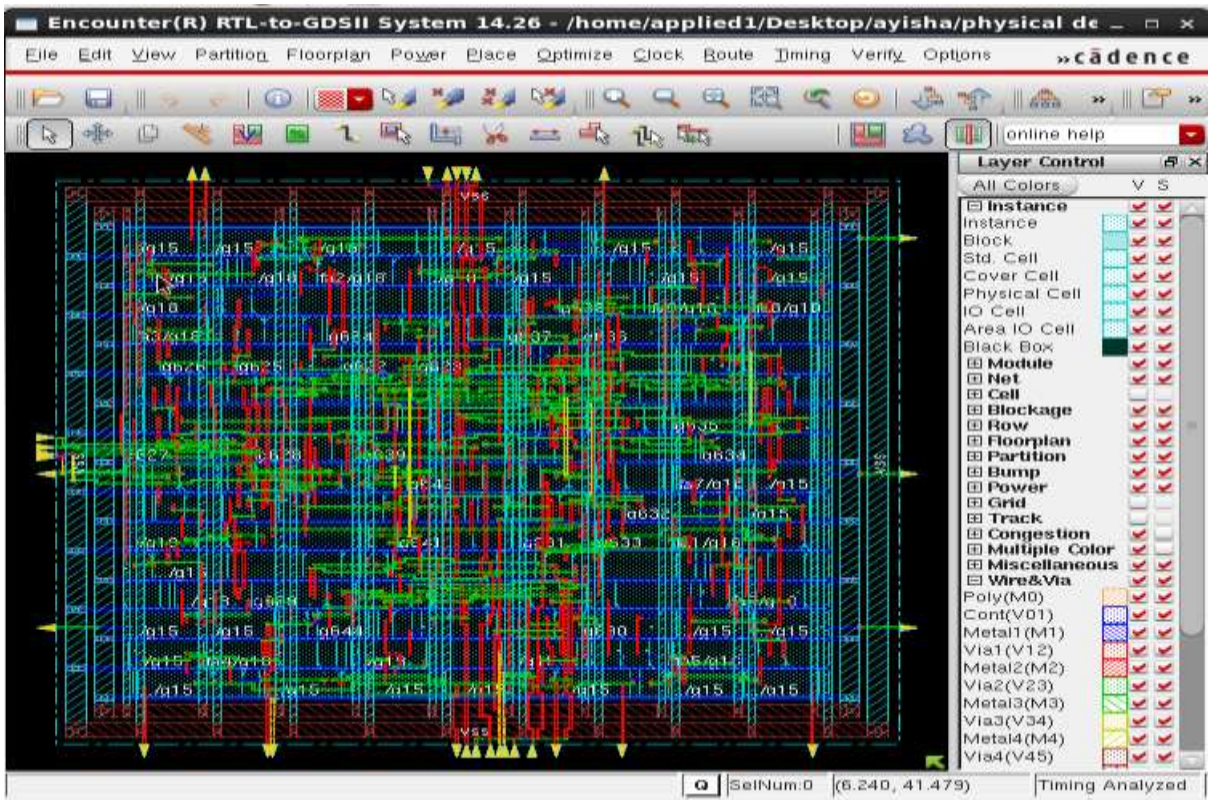


Fig7:simulated output

Layout



VII.CONCLUSION

The proposed approximate 16 bit multiplier produce less error output and delay. It can be used in many of the applications. In the future work try to reduce the error and number of gates used.

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