International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.07, April 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

DEVELOPMENT AND IMPLEMENTATION OF TEST SYSTEM FOR BASEBAND DATA HANDLING SYSTEM

Vedant Rajendra Shinde[1], Raksha T[2],

Sreeram R[3], Imad Ul Islam[4], Dr. SN Prasad[5]

[1, 2, 3, 4, 5] *School of Electronics and Communication Engineering, REVA University, Bangalore, (India)*

ABSTRACT

Baseband data handling system is a vast system which is used to transmit different payload data from the satellite and variousfunctionalities are implemented like data compression, data formatting, data encryption and channel coding technique. This paper focuses on the data packetization unit, where a test system is developed in which space packets are generated by creating and combining a header with different types of the payload data.

Keywords - *Baseband data handling system, data packets, test system, VHDL, Xilinx*

I.INTRODUCTION

The Indian Remote Sensing (IRS) satellite revolves around the earth to fetch information. The data is captured with help of payloads like Panchromatic (PAN) and Multi-spectral (MX) cameras of IRS satellite. The BDH system performs functions like compression, formatting, encryption and channel coding. With rising time in technology, payloads are generating data packets and sending it to BDH system for further processes. The data packets are generated by adding a header to payload data. The packet header consists of Application process ID (APID), packet count, and packet length.The payload data varies according to the type of a payload and its application [1].

A test system is created using Xilinx software in which VHDL code helps in stimulating data packetization process which is carried out in payloads. The payload data used for test system aredifferent types of counters like up counter and down counter. The output of the test system is clock, space packets, and data valid i.e. header combined with data, this output is obtained using input clock, reset, enable and counter signals.

II. RELATED WORK

2.1 Baseband Data Handling System Using LEON3FT Processor

The payload data enters the Baseband Data handling (BDH) system from different types of payloads through various payload interfaces such as ECL, LVDS and TTL. The whole BDH system is implemented using separate processor attached with FPGA [1].

2.2 Design And Implementation of Payload Data Handling Based on Field Programmable Gate Array

The payload data handling system is designed toconcentrate on two modules, CCSDS and Reed-Solomon encoder module.The test system is created with the help of VHDL code and further tested by using simulation environment. After successful compilation, this test system is synthesised on to the hardware [2].

2.3The Architecture of Cost-effective, Advanced, High Data Rate Baseband Data Handling System and realization for High-Resolution Remote Sensing Satellites

This paper focuses onreducing the cost parameter, achieved larger data transmission with respect to time and acquiring enhanced pixels images captured by payloads [3].

2.4 Test station for CCSDS based data handling systems of mini satellites

Various test stations are placed in order to test the communication of the baseband data handling system. Different types of systems are used to test the complete base band system. In order to acquire various satellite missions these interfaces are combined with the other small systems [4].

2.5 Design & realization of multi mission data handling system for remote sensing satellite

This paper defines the changes that are made to the programs and software for the flexibility of the different types of satellite missions. This type of approach saves time and cost instead of using many different types of hardware and software elements for the different applications [5].

2.6 Design and implementation of IEEE 802.16 baseband system on FPGA

This paper defines the Baseband system delay in order to attain higher data transmission. As channel coding is undergone, the coded signal gets encrypted and transmitted in the X Band region. The data packets are synchronized with the help of frame synchronization marker [6].

2.7 An architecture of baseband data handling system for deep space mission and realization for Mars Orbiter Mission

This paper explains the functionalities of a baseband data handling system. Functionalities like data compression, data formatting and data encryption are necessary for the processing of data and further transmission to the ground station. Different types of data transmission and data reception are carried out in the baseband data handling system for deep space mission [7].

2.8 An FPGA based implementation baseband and pass band modulation for wireless transmitters

This paper explains the synthesis process of the VHDL codes to the practical hardware system. Any problem encountered in the practical hardware can be addressed and corrected once the FPGA is ready. Processes such as channel coding, encryption, data formatting etc. are implemented into the hardware [8].

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.07, April 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

III. PROPOSED WORK

A test system is a simulator which provides a virtualized environment, created or developed with the help of Xilinx software by using VHDL code. The input to a system is a master clock which controls the entire system with rising edge of the event. Another input signal is master reset which controls the system when a signal is high and when the signal is low, the system turns off. The required VHDL program consists of a 16-Bit master counter, 11-Bit counter, 3-Bit counter, master clock signal, the master reset signal and two enable signals. The master reset signal initializes the entire system to the initial state. The 11-Bit master counters increment upon power-on condition until a particular specified range.Once the master counter reaches this particular range, it completes one cycle and thus initializes to the initial starting range. Both the enable signals to depend on a particular range of the 11-Bit master counter, to either be high or low. The two enable signals, reset signal and the clock signal areresponsible for the control of the 3-Bit counter and the 10 –Bit counter respectively. The 10-Bit and the 3-Bit counter operate within a specified range with respect to the master reset, master clock and they enable signal. The 10-Bit counter used here represents the data. The 3-Bit counter acts as a header where the Application Process ID (APID), sequence number and packet length are represented. The APID is pre-defined where the source address is present.The output of the system is master clock, space packets which are basically header combined with data and last output signal is called data valid i.e. when data valid signal is high it transfers the data packets and when data valid signal is low it waits for next cycle to transfer the other data packets.

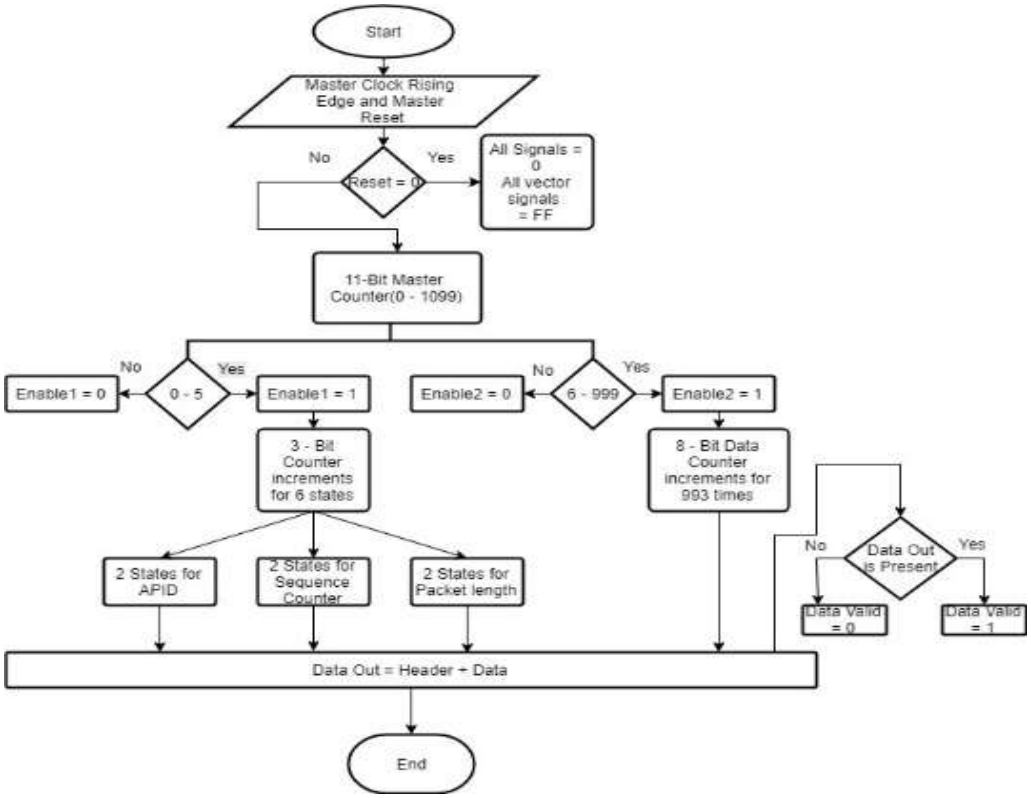

Fig.1. Architecture of VHDL code

The above flowchart represents the proposed work in detail. The VHDL codes are compiled and executed giving the expected waveform of three cycles within the time frame of 75,000ns.

IV. RESULTS

The test system is successfully developed with help of Xilinx software, where stimulator is helping us to study the behaviour of data packetization process occurring in the payload. The output of the test system is master clock, space packets, and data valid. The space packets consist of a header and the data. W98+hen data valid signal is high, space packets are transferred and when a signal is low, packets are withheld until next cycle. The following waveforms are obtained only during the rising edge of the master clock and when master reset signal is high.

4.1 WAVEFORMS

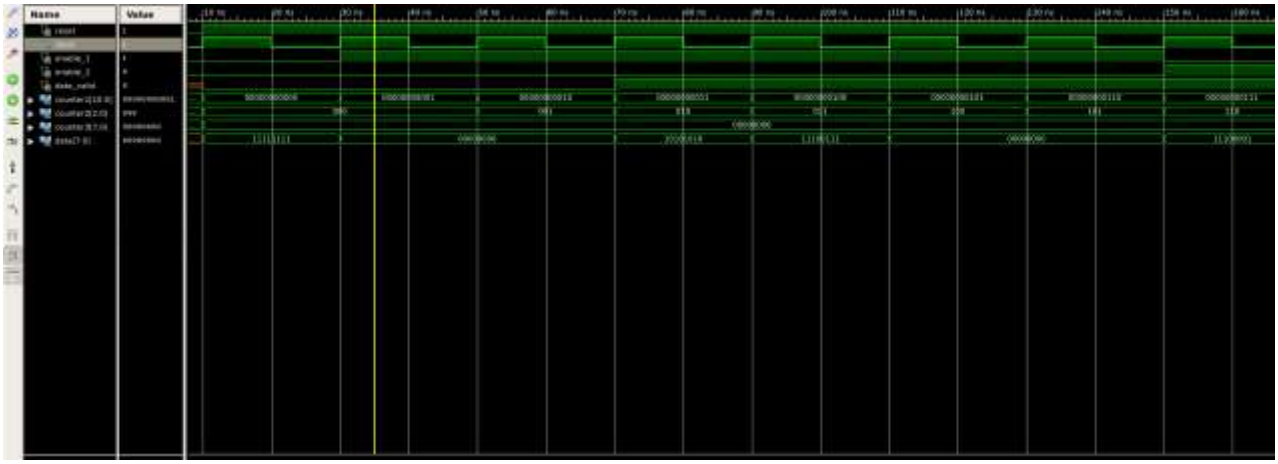

Fig.2. Header of the 1st cycle

It is divided in three parts i.e. APID, packet count, packet length. Each of three parts take two state. The two states are combined to give the output of either the APID or packet count or packet length. Each of the header parts are 16 bit, which are further divided in two part and are placed in two states. The header is significant when enable 1 and 3 bit counter are functional.

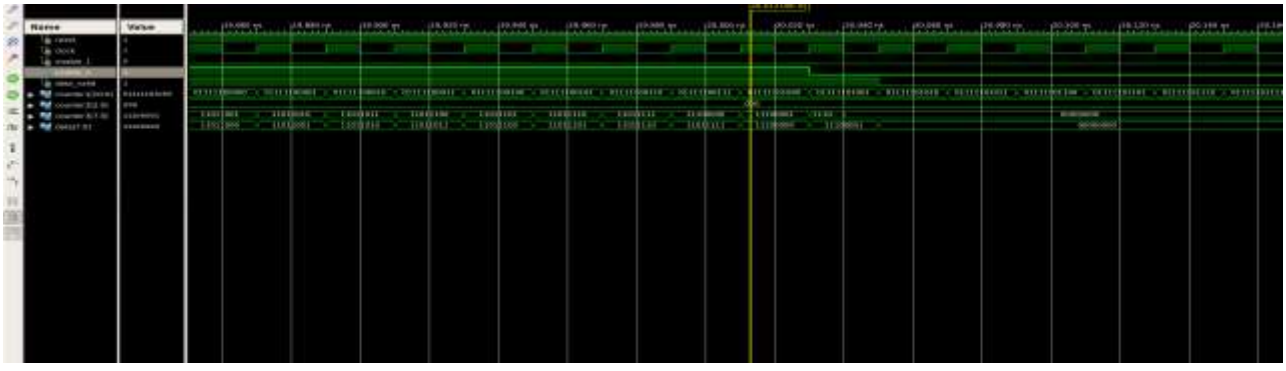

Fig.3.–Data end of 1st cycle

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.07, April 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

The 8 bit data is used and made to be functional for 993 states. Different type of data can be fed by using enable 2 as control signal. After the specified range of 1st cycle the data goes low, giving the time frame before the initialisation of the second data packet cycle.

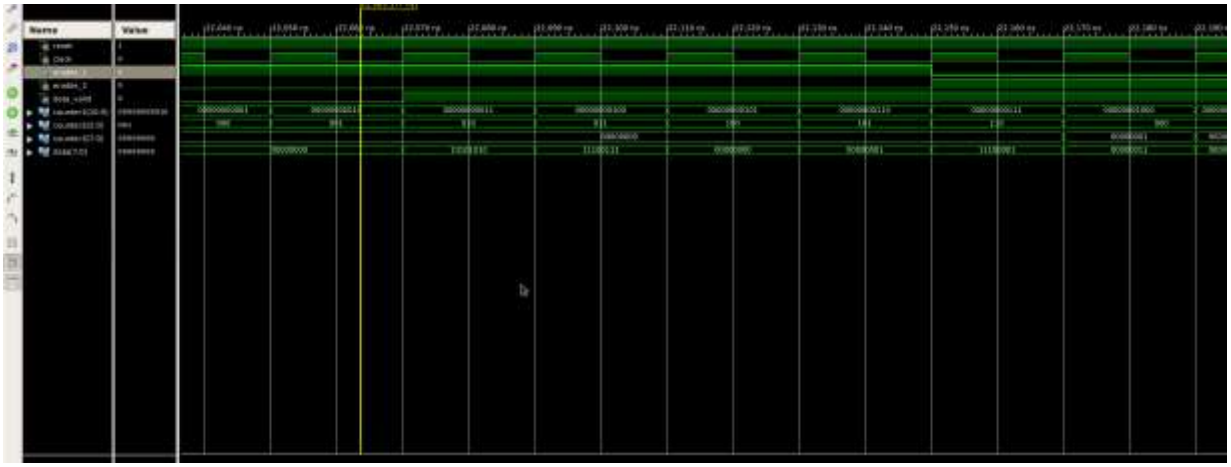

Fig.4. Header of 2nd Cycle

The master counter goes back to initial zero state after reaching the 1099 state. The packet count is increment by 1 bit in 2nd cycle.

Fig.5.Data end of 2nd cycle

The 8 bit data is used and made to be functional for 993 states again. After the specified range of 2st cycle the data goes low, giving the time frame before the initialisation of the third data packet cycle.

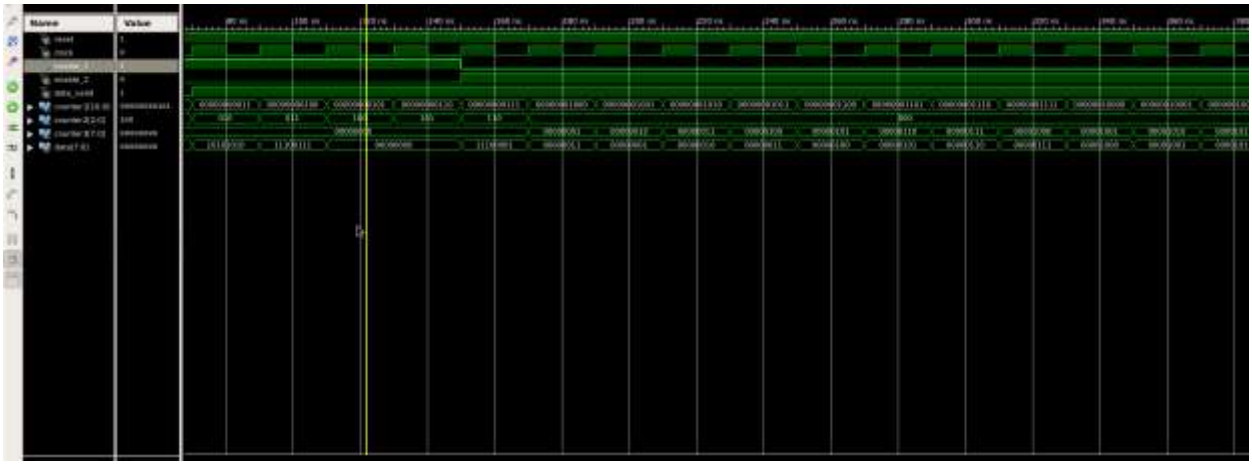

Fig.6. Header and Data of 1st cycle

The header becomes low immediately when 3 bit counter stops incrementing due to the enable 1 signal. As soon as enable signal goes high, the data is fed or incremented until the specified range of the data packet.

V. CONCLUSION

In this paper, thetest system of data packet generation in a payload is explained and also developed with the help of VHDL code using the stimulator environment created by Xilinx software. It helped us in studying the nature of BDH system and transmission of space data packets from space – to – space or space – to – ground via RF system. Later these space packets go for further process like compression, encryption etc. and stored in solid state recorder for future references.

REFERENCES

[1]APA Arun. N, Dr. S Revathi, May 16 *Volume 4Issue 5*, "*Baseband Data Handling System Using LEON3FT Processor"*, International Journal on Recent and Innovation Trends in Computing and Communication (IJRITCC), ISSN: 2321-8169, PP: 66 – 71

[2] Roza, Widya & El Amin, Deddy & Nasemudin, Eriko. (2014). *Design and implementation of payload data handling based on field programmable gate array*. 48-54. 10.1109/ICARES.2014.7024397.

[3] Sahul M.P.V, Ankit Agarwal, Somasundaram.S, Gaurav Upadhyay, Thenmozhi Selvi.K, Sura P.S, Subramanya Udupa, *Architecture of cost-effective, advanced, high data rate baseband data handling system and realization for high-resolution remote sensing satellites*, 2017 4th International Conference on Power, Control & Embedded Systems (ICPCES).

[4] K.H. Jeeja, Chayan Duta, Lalitkrushna Thakar, P S Sura, M. Vanitha, *Test station for CCSDS based data handling systems of mini satellites.* Advanced Communication Control and Computing Technologies (ICACCCT), 2012 IEEE International Conference.

[5] Lalitkrushna Thakar, Chayan Dutta, P S Sura, S Udupa, *Design & realization of multi mission data handling system for remote sensing satellite.* Advances in Computing, Communication and Informatics (ICACCI), 2016 International Conference.

[6] Chen Gu, Xu Li, *Design 998and implementation of IEEE 802.16 baseband system on FPGA,* Communication Technology and Application (ICCTA 2011), IET International Conference.

[7] K H Jeeja, Keeerthi K, Lakshmi A, Shantala S H, Jothy Soman, P S Sura, Valarmathi N, *An architecture of baseband data handling system for deep space mission and realization for Mars Orbiter Mission,* Advances in Computing, Communications and Infomatics (ICACCI), 2015 International Conference.

[8]Saad Zafar, Sushant Kataria, Abhishek Sharma, *An FPGA based implementation baseband and passband modulation for wireless transmitters* Electronics and Communication System (ICECS), 2014 International Conference.