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# MODIFIED DLL BASED CLOCK GENERATION FOR LOW POWER SYSTEM ON-CHIP

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## ABSTRACT

*A 4.5 Mill Watti, 0.01148 MM-2 frequency multiplier based on mixed-mode delay-locked-loop (DLL) in 65 nm CMOS technology is presented in this paper. The operating frequency range is between 100 and 150 MHz which enables to produce output signals in the frequency range from 4 to 6 GHz. NAND-based delay cells are used in the digital part of the delay line due to their wide operating frequency range and small intrinsic delay. The analogue part of the delay line is based on the inverter delay chain with biasing circuit. It was added into the system to overcome the resolution problem and improve jitter performance. The total locking time changes from 10 to 14 clock cycles based on the operating frequency. The simulated peak-to-peak jitter is 21 ps and 1.95 ps for the generated clock operating at 5 GHZ and output clock of DLL operating at 125 MHz respectively.*

***Keywords*** **:** ***Delay Line , Delay Chain, Frequency Multiplier ,Jitter, Resolution***

## I. INTRODUCTION

In high-performance system on chip (SoC), more than one frequency generation block is necessary to derive the various clocks and LO frequencies. These multiple frequencies are generated with Phase Locked Loops (PLLs) due to the given good phase noise and output spectrum. However, PLLs have some drawbacks which makes it unstable and difficult to design like high order loop filter characteristic and jitter accumulation. For conventional PLLs, it is common to use LC-type voltage controlled oscillators (VCOs) which occupy large area and consume high power. That is why using multiple PLLs is not very practical under these circumstances. Instead of PLLs, Delay Locked Loops (DLLs) are alternative for frequency generation. Unlike PLLs DLLs do not accumulate jitter over each clock cycle and have lower power consumption. It is the first order system which makes it easy to design and stable in most cases. Since DLLs occupy small area, multiple of them can be used in complicated systems without area penalty. The PLLs have some pulling effect between their Voltage Control Oscillators which makes difficult to use multiple of them in the same design but in case of DLL this effect is avoided due to the absence of VCO. The DLL is mainly classified into three different categories which are analogue, digital and mixed-mode DLL. The typical analogue DLL has voltage controlled delay line (VCDL) to delay the input signal and create equidistant multiple phases which can be used to generate higher frequency.

## II EXISTING TECHNIQUE

Delay Lock Loop based clock generator is consists of a DELAY LOCK LOOP core and the proposed frequency multiplier. To enhance the lock time, which is an vital design parameter in the clock generator, a dual-edge triggered phase-detector-based DELAY LOCK LOOP core is adjustable. Same as previous frequency multipliers, the proposed frequency multiplier also consists of a pulse generator, multiplication ratio logic circuit controller, and an Edge Combiner. The Dual Edge Triggered, Phase-detector characterises both the raising and the falling edges of Reference CLK, Delayed CLK and output CLK, Delayed CLK, which are the duty cycle recovered clocks of Reference CLK and Output CLK using the duty-cycle maintainer. The ***DELAY LOCK LOOP*** is locked within (300) three Hundred clock cycles in all process–voltage–temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks phase 20 to 25 and phase 20 to 25. Using the 32-phase differential clocks, the pulse generator makes pulses Phase G 20:25 and Phase G 20 to 25 for positive- and negative-edge generation. The multiplication-ratio control logic selects appropriate pulses from Phase-G 0:31 and Phase-G 0:31 and generates MC-*P*,0:15 and MC-*N*,0:15 according to the multiplication ratio control signal. Finally, the high-speed and highly reliable edge combiner generates one multiplied clock using all the outputs of the multiplication ratio control logic. Hence the number of multiphase is 20 to 25, the maximum multiplication ratio is 16.

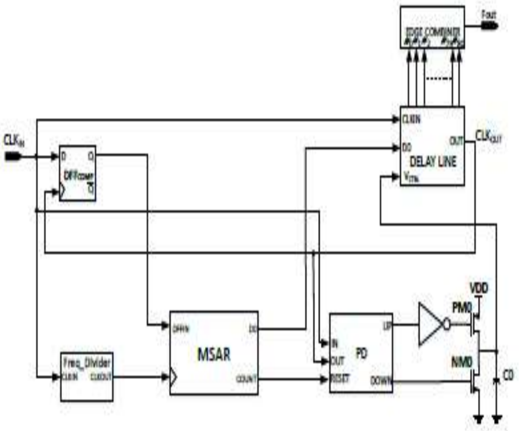


**Fig.1: Block diagram of the proposed mixed-mode DLL**

## III HARDWARE IMPLEMENTATION

The digital part consists of a modified successive approximation register (MSAR) [2], a D-type flip-flop (DFF), frequency divider, and digitally controlled delay line (DCDL) for coarse tuning, the analogue part has a Phase Detector (PD), a Loop Filter, Voltage Controlled Delay Line (VCDL) for fine tuning. The edge combiner is the last part of this system which combines all phases coming from the delay line to generate high frequency output signals. When the input signal (CLKIN) rises, the phase difference between the output of the delay line (CLKOUT ) and CLKIN is compared by the DFF and the result is sent to the MSAR

to determine its digital control bit D0 to control the delay time of the DCDL in each delay cell for coarse tuning. After the digital part has finished, the Count signal rises to enable the PD. PD determines the remaining phase difference between CLKOUT and CLKIN, and sends UP or DOWN signal to the charge pump. These signals are used to charge or discharge the loop filter capacitor to determine Vctrl which adjusts the total delay time of the VCDL for fine tuning. When the phase difference between the two signals becomes so small that it falls into the dead-zone of the PD, it stops responding and Vctrl stays constant and the locking point is reached. All 80 equidistant phases are sent to the edge combiner to generate the output frequency.

### 3.1 Modified Successive Approximation Register (MSAR)

MSAR is the main controller of the digital part of the proposed DLL. It is used to control the DCDL. The MSAR consists of one MSAR unit which is assigned to single control bit (D0). The complete MSAR architecture is shown in Fig. 2. The other one OR gate and two DFFs are used to enable or disable the MSAR unit and trigger COUNT signal which will be used as a RESET function to enable PD. In the MSAR unit, which is shown in Fig. 3, the locking process is divided into two parts:

At first, while the Enable signal is still 0, the shift signal which is connected to VDD

in this case keeps the AND1 gate at logic 1 because OUTINVT and the inverted version of the Enable signals are still 1. Naturally, the NOR gate responses with logic 0. The output of the NAND1 gate is always 1 as long as Enable is 0. The output of the NOR gate keeps out of NAND2 gate at logic 1 which will be used as a data signal by the DFFMSAR. When the Clock signal rises, the output of the DFFMSAR becomes 1 and Comp which is sent by DFFCOMP by comparing CLKOUT and CLKIN is checked to whether the output should be kept at 1 or changed to 0. If Comp signal is at logic 1, that means output clock lags the input one so that the output of the DFFMSAR should be changed to 0 to decrease the total amount of the delay time in the DCDL. If Comp is 0, the input clock lags the output clock. Thus, control bit will remain the same at 1. After Enable is signal pulled up to VDD, the Comp signal will be disregarded and the output will be fixed as long as the input clock does not change. B. Phase Detector (PD) The Phase Detector (PD) is one of the most important parts of the proposed DLL. As shown in Fig. 4, the proposed architecture is a modified version of a conventional PD where the RESET signal comes from the MSAR as a COUNT signal to enable it. Until the RESET signal is pulled to VDD, the UP and DOWN signals are kept at logic 1 and 0, respectively. In that way Vctrl is kept at

VDD via the charge pump and the loop filter capacitor which gives the minimum delay time in the VCDL. After the PD is enabled, Vctrl starts decreasing to adjust the total delay time to find the correct locking point.Since the sensitivity of the PD determines the phase difference between the input and output clocks, the dead-zone of it is minimised to obtain good output jitter performance. Based on layout-extracted simulation results, the dead-zone of the PD is less than 1 ps for all four-corner cases.

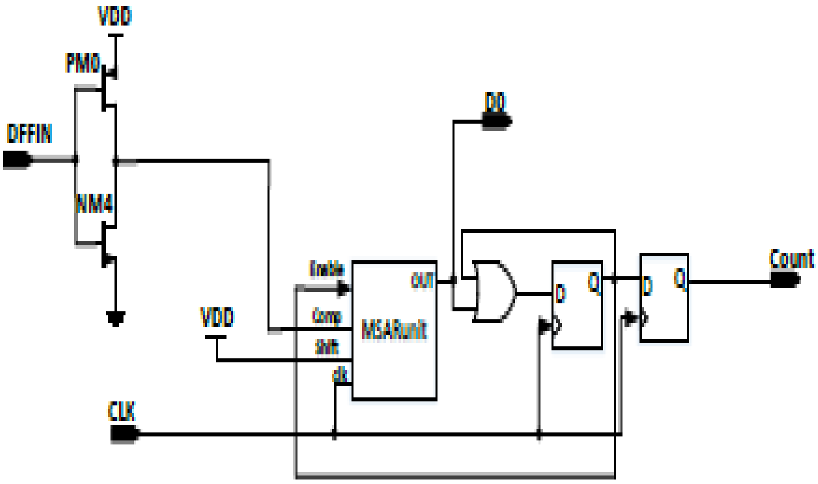


Fig.2: Schematic of the designed MSAR

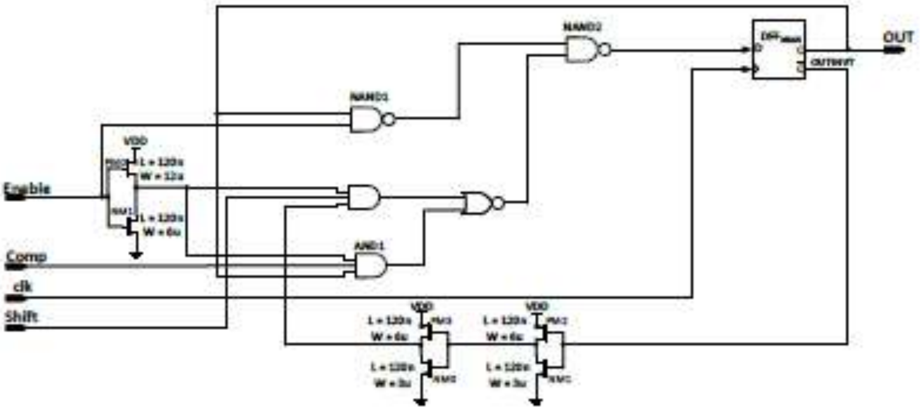


Fig. 3: Schematic of the MSAR unit

### 3.2. Delay Line

In terms of design, the delay line is the most critical part of the proposed DLL. It consists of 80 delay cells which gives equidistant phases to the edge combiner to generate the higher frequencies. The cell structure is shown in Fig. 5. Each cell has two different parts: a digital and analogue part i.e the DCDL and VCDL, respectively. For the DCDL part, a NAND-based delay line is preferred due to its advantage in terms of wide frequency range and small intrinsic delay time compared to an inverter-based one. Since one of two inputs of the NAND gates is at

logic 1, When the control bit (D0) is 0, both of them start acting like a common inverter. In this situation, CLKIN follows the shortest path and the total delay will be two NAND gates and it is called minimum delay time. The rest of the NAND gates are not counted so they can not add any additional delay on CLKIN. If D0 is pulled up to 1 (VDD), since the input of the first NAND Gate is kept at logic 0 due to the inverted version of D0, its output will be at logic 1 and hence CLKIN is routed through the longest path which results in more than 3 times of the individual delay time of a single NAND gate. This delay directly depends on the number of NAND gates that are placed in each part. A larger number leads to a wider operating frequency range. The total delay time of the complete digital parts cannot exceed the period of the input signal. Therefore, there is always a residual phase difference between the input and the output clocks after the digital part is settled. Now the analogue part starts working to adjust the correct delay time to find the exact locking point. Vctrl controls the delay of the inverters in each cell via the biasing circuit. After the correct Vctrl is settled, the total delay time for one complete cell will be equal to half a period of the output frequency generated by the edge combiner.

## IV SIMULATIONS

### 4.1 SYNTHESIS REPORT

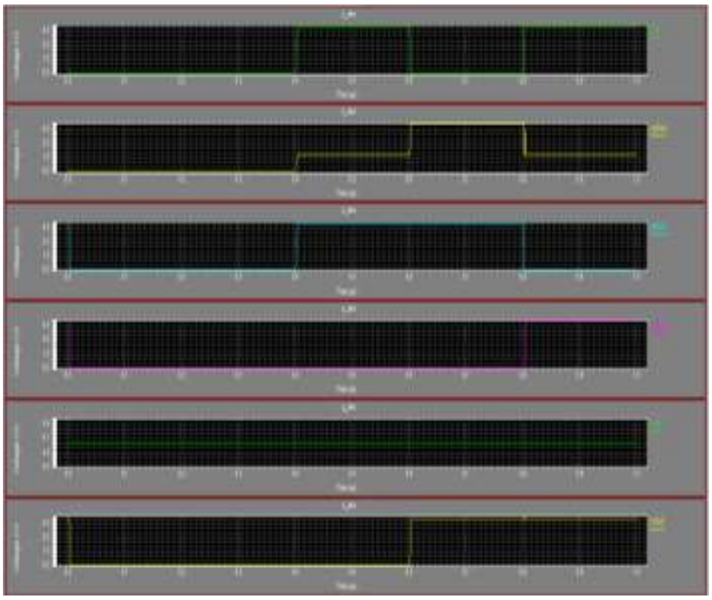


Fig.4: Simulation Output

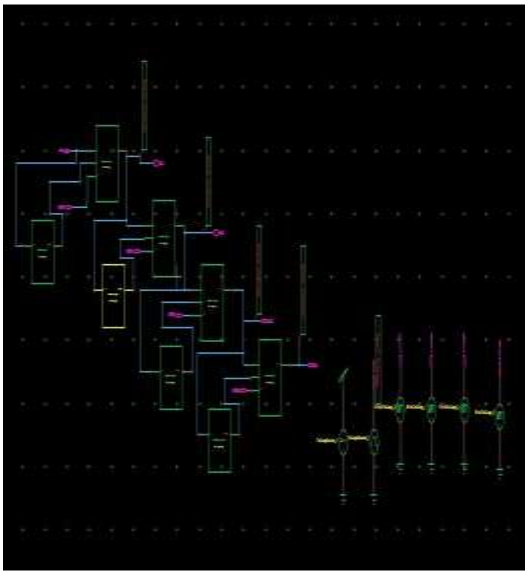


Fig.5: Schematic Design

## 4.2 SIMULATION REPORT

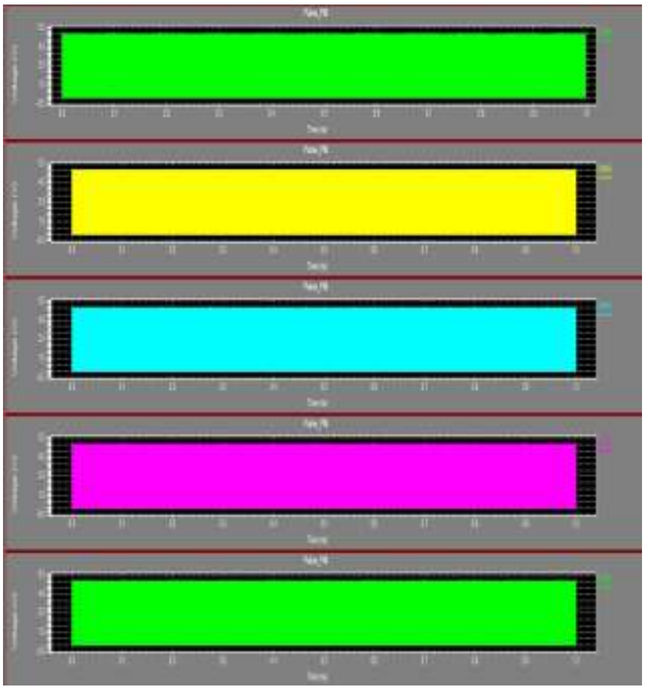
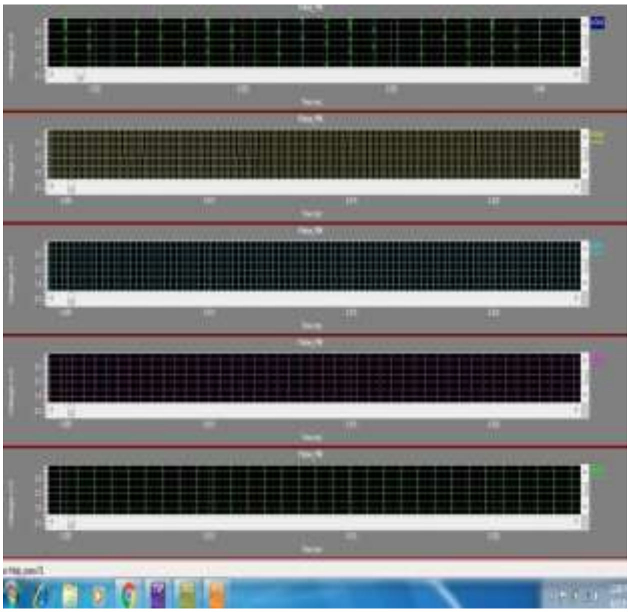


Fig.6: Simulation Output



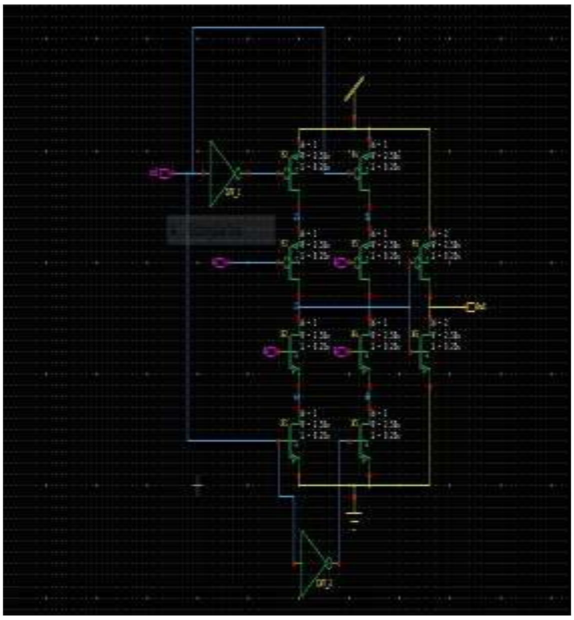
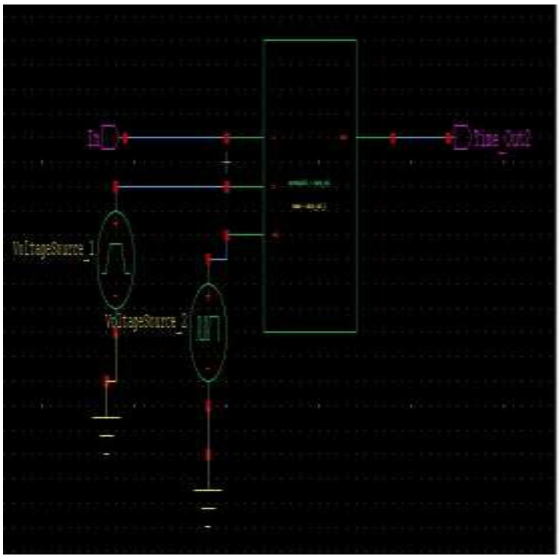


**Fig.7: Simulation Output   Fig.8: Internal Schematic View**



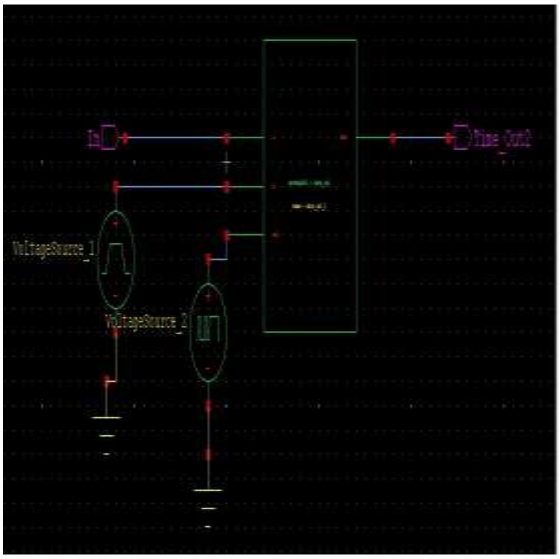


**Fig.9 Internal Schematic View   Fig.10: Internal Schematic View**

## V POWER RESULTS

Total Power from time 0 to 0.001

Average power consumed -> 5.314303e-004 watts

```
Max power 9.686614e-002 at time 2.30045e-009

Min power 6.128086e-010 at time 0.00081622

* END NON-GRAPHICAL DATA

* Parsing                   0.03 seconds

* Setup                     0.16 seconds

* DC operating point          0.50 seconds

* Transient Analysis        487.44 seconds

* Overhead                   0.73 seconds

* ----------------------------------------

* Total                   488.86 seconds

* Simulation completed
```

## VI .COMPARISON

| **Parameter** | **Existing** | **Proposed** |
|---|---|---|
| **vdd** | **1.2v** | **1.2v** |
| **Multiplication Ratio** | **16** | **64** |
| **Frequency** | **1.5Ghz** | **6Ghz** |

**Table 1 : Comparison chart**

## VII . CONCLUSION

The proposed mixed-mode DLL achieves low power consumption, small area and good jitter performance because of the combination of both analogue and digital part of DLLs. While MSAR enables to achieve short-locking time and wide operating frequency with DCDL, analogue voltage (Vctrl) gives good resolution in overall delay line by controlling VCDL for fine tuning.The proposed system occupies 0:011 48mm2 in 65nm CMOS technology. It consumes 4:5Mill Watti power and can reach the lock state around 10 clock cycles. Its peak- to-peak jitter is 21 ps for 5 GHz generated output frequency (FOUT ).

## REFERENCES

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