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THD COMPARISON USING DIFFERENT PWM TECHNIQUES FOR SINGLE PHASE ELEVEN LEVEL INVERTER

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ABSTRACT

Implementation of an eleven level inverter is designed. Here different PWM methods are employed that is in phase disposition pulse width modulation (IPDPWM), phase opposition pulse width modulation (PODPWM), alternative phase opposition disposition pulse width modulation (APODPWM) and variable frequency pulse width modulation (VFPWM) and calculated the total harmonic distortion .By comparing the THD which gives less THD is chosen to be the most effective PWM methodology for single phase eleven level inverter. The simulations of an eleven level inverter with different PWM methods have been done in MATLAB/Simulink.

Keywords: *Alternative phase opposition disposition (APOD), In phase disposition (IPD), Pulse Width Modulation (PWM), Phase opposition (POD), Total Harmonics Distortion (THD), Variable frequency* ***(VF)***

I.INTRODUCTION

Power electronics device plays an important role in the conversion and control of electric power, especially to extract power from renewable energy sources like, tidal energy, photovoltaic array and wind energy. DC power can be converted to ac power with the help of inverters it may be (single phase or three phases). By using conventional bipolar inverters we can produce alternating staircase but these waveforms produce higher amount of harmonics. To eliminate this, the multilevel inverters (MLI) were developed [1]. Basically, inverter that converts DC power to AC power at desired output voltage and frequency. A drawback of inverter is less efficiency, high THD, and high switching losses. To overcome these drawbacks, we are going for multilevel inverter. The duration multilevel structure instigated with the three-level converter. The conception of multilevel converters has been announced since 1975. Cascade multilevel inverter structure was initial recommended in 1975, these days multilevel inverters are used for high voltage and high power applications. Modular multilevel converters have abundant potential in high power applications, like dc interconnections, Off-shore, and dc power grids wind power generation are in most of tangible power flow control and high potency power conversion so as to cut back each their environmental impact and their operating costs [2].

Multilevel inverters are considered today as the state-of the- currently considered as an improved industrial resolution for high dynamic performance and power-quality stringent applications, covering a good power vary. Cascaded H-bridge structure multilevel inverters are been researched for high voltage applications since it has advantages in number of components, high reliability, and modularity. One of the demerits of cascade multilevel inverter is that as the number

of level increases, the number of H-bridges also increases. These types of inverters are appropriate for high voltage and high power applications due to their ability to synthesize waveforms with higher harmonics spectrum. [3], [4]. The number of applications of multilevel power inverters in the field of medium and high voltage has increased. This gives birth to greater attention on multilevel topologies. The most common multilevel converters use symmetric topologies such as DCMC (diode clamp multilevel converters), FCMC (flying capacitor multilevel converters), and CCMC (cascade cell multilevel converters). Asymmetrical structure of multilevel inverters have received increasing attention as a result of its attainable to synthesize voltage waveforms with reduced harmonic content, even employing a few series-connected cells [5].

.Conventional pulse width modulation techniques (PWM) employed in symmetrical inverters could be employed in asymmetrical inverters. The foremost widely used techniques for implementing the pulse width modulation (PWM) strategy for multilevel inverters are sine-triangle PWM (SPWM) and space vector PWM (SVPWM). The thought of power quality and power-electronics based mostly custom power devices are of utmost importance today. A large variety of nonlinear loads are used in the industry for various operations which in turn induce harmonic distortion and reactive power issues within the supply network [6-7]. Harmonics in the supply are responsible for various adverse effects like transformer losses, power factor reduction, measurement errors, heating losses, and reduction in efficiency. They also affect the other consumers linked to the same supply network [8]. There are many inverter topologies within which cascaded inverter have some advantages compared to other type of multilevel inverters such as reduced harmonics however they have drawbacks also such as many heat losses, a lot of switches, high cost [9-10]. PWM techniques are used gating pulses. Those PWM techniques are In Phase Disposition, Phase Opposition, Overlap Carriers, and Varying Frequency PWM techniques. The proposed configuration has several advantages, i.e., reduced cost reduced harmonics, pure sine output, reduced gate control, very less heating losses [11-13].The foremost issues is associated with multilevel inverters are the harmonic content present at the output of the inverter and the requirements of large number of switches, which can increase the switching losses, thereby reduce the efficiency and overall cost of the inverter is augmented, so here completely different PWM methods are applied and based on the THD result which gives less total harmonic distortion is chosen to be the most effective PWM methodology for inverter.

II. MODULATION TECHNIQUES

2.1. In Phase Disposition Level-Shift PWM Technique (IPDPWM)

In this technique the carrier waves are arranged in phase. These carrier waves are compared with reference wave. If all carriers are selected with the same phase, this technique is known as In Phase Disposition technique. It is generally accepted that this technique gives rise to the lowest harmonic distortion in higher modulation indices when compared to other disposition technique. The rules for the phase opposition disposition method, when the number of level N = 11. The N –1 = 10 carrier signals are arranged. The carrier waveforms of this technique are illustrated in Fig.1

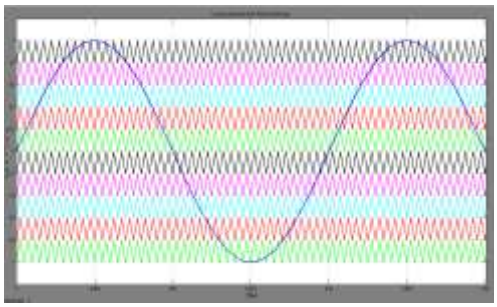

Fig. 1: In Phase Disposition Level-Shift PWM Technique (IPDPWM)

2.2. Phase Opposition Disposition PWM (PODPWM)

The Phase Opposition Disposition (POD) technique, having the carriers above the zero line of reference voltage out of phase with those of below this line by 180 degrees as shown in Fig.2.Compared to the PD method, this technique has better results from the point of view of harmonic performances in lower modulation indices. The rules for the phase opposition disposition method, the number of level N = 11. The N –1 = 10 carrier signals are arranged so that all carrier waveforms above zero are in phase and are 180° out of phase with those below zero.

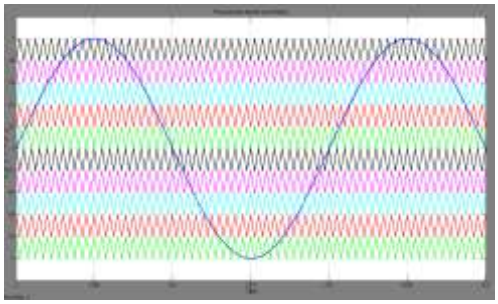

Fig. 2: Phase Opposition Disposition PWM (PODPWM)

2.3. Alternate Phase Opposition Disposition PWM (APODPWM)

Alternative Phase Opposition Disposition (APOD) technique each carrier of this technique is phase shifted by 180° from its adjacent one. This technique gives almost the same results as the POD technique. The major differences are the larger amount of third order harmonics which is not important because of their cancellation in line voltages. This technique results in a better THD for line voltages when comparing to the POD technique. In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180°. The carrier waveforms of this technique are illustrated in Fig.3.

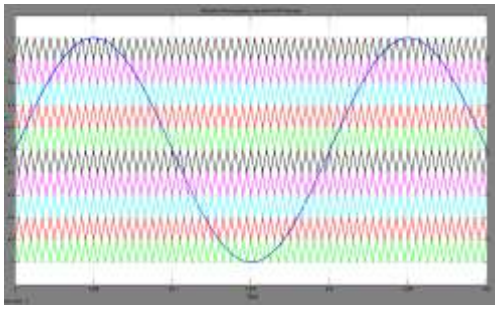

Fig.3: Alternate Phase Opposition Disposition PWM (APODPWM)

2.4. Variable Switching Frequency PWM (VSFPWM)

In this technique ten carrier signals are of different frequency but having same amplitude as shown in Fig.4. Out of ten signals five are on the positive phase and other five are in negative phase. Ten carrier signals having different frequency is comparing with reference signal.

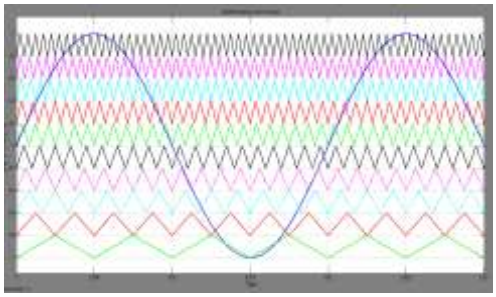

Fig.4: Variable Switching Frequency PWM (VSFPWM)

III.MULTILEVEL INVERTER

The inverter structure consists of twenty switches, ten upper and ten lower switches. The typical structure of a MMC is shown in Fig.6. Each SM is a simple cell composed of two IGBT switches (T1 and T2). The configuration with T1 and T2 both ON should not be considered because it determines a short circuit. Also the configuration with T1 and T2 both OFF is not useful as it produces different output voltages depending on the current direction. In a MMC the number of steps of the output voltage is related to the number of series connected SMs.

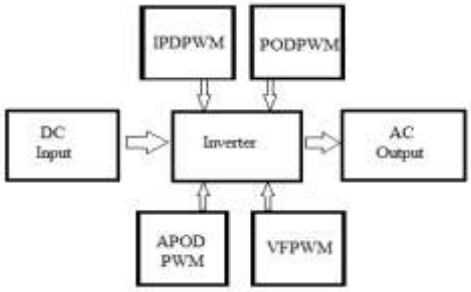

Fig 5: Block diagram of the inverter

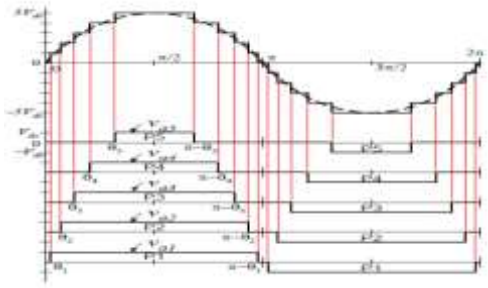

Fig 6: Eleven level output voltage waveform indicating voltage levels

The eleven level inverter consists of different voltage levels of 5vdc, 4vdc, 3vdc, 2vdc, vdc, 0,-vdc,-2vdc,-3vdc,-4vdc and -5vdc.Wavefoem of these voltage levels is shown in Fig.6.The operating regions and the voltage levels of eleven level inverter is depicted in Table 1.

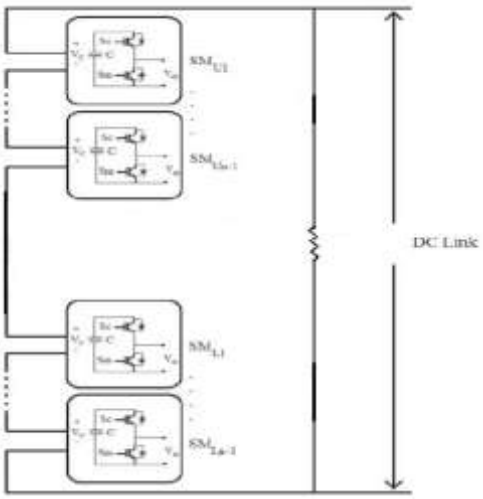

Fig 7: Single-phase MMC inverter structure.

Table 1: Operating regions of eleven level inverter

Voltage level	Status	Gates	Vout
1	Vr>=Vc1	U1a.U1b	5Vdc
2	Vr>=Vc2	U2a,U2b	4Vdc
3	Vr>=Vc3	U3a,U3b	3Vdc
4	Vr>=Vc4	U4a,U4b	2Vdc
5	Vr>=Vc5	U5a,U5b	Vdc
6	Vr>=Vc5,Vr>=Vc6	U5a,L5a	0
7	Vr>=Vc6	L5a,L5b	-Vdc
8	Vr>=Vc7	L4a,L4b	-2Vdc
9	Vr>=Vc8	L3a,L3b	-3Vdc
10	Vr>=Vc9	L2a,L2b	-4Vdc
11	Vr>=Vc10	L1a,L1b	-5Vdc

Inverter consists of twenty numbers of switches ,ten switches are considered for positive cycle and remaining ten switches are used for negative cycle. As number of levels increased the total harmonic distortion will be reduced in the system output. The output of the inverter consist different voltage levels these are given in Table 1.

IV. SIMULATION RESULT

Generation of PWM pulses

No of carrier pulses = N-1

N=number of levels for Inverter N=11

N=11-1=10 carrier waves are required to get the eleven level output.

$$F = \frac{1}{T} \quad T = \frac{1}{F} \qquad 1$$

For sine wave frequency is 50Hz

$$T = \frac{1}{50} = 0.02sec$$

For carrier wave frequency is 2 KHz

$$T = \frac{1}{2000} = 500e^{-6} \quad T = 500e^{-6} * 40 = 0.02sec$$

IPDPWM, PODPWM, APODPWM

Carrier wave amplitude =0.2V

Ten carrier wave Frequency=2000Hz

VFPWM

Carrier wave amplitude =0.2V

Frequency=200,400,600Hz,800Hz,1000Hz,1200Hz,1400Hz,1600Hz,1800Hz,2000Hz.

Inverter

Number of switches =20,Input DC Voltage for sub circuit V=200V ,Output AC voltage of inverter=1000V

R=25Ω

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_rms}^2}}{V_{fund\_rms}} \qquad 2$$

Where $V_{n\_rms}^2$ = is the RMS voltage of the nth harmonic

V_{fund_rms} = *is the RMS voltage of the fundamental frequency*

Eleven Level Inverter

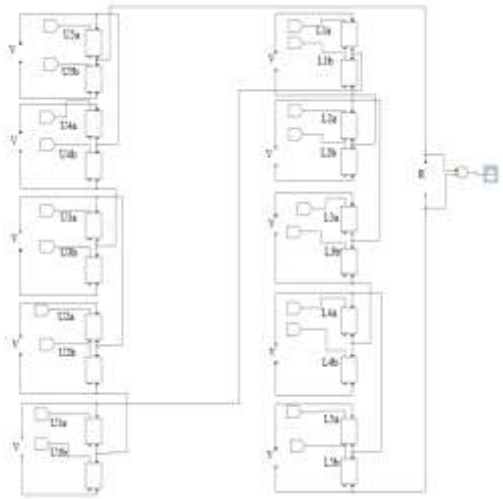

Fig.8: Simulink model of eleven level inverter

In this model, this consists of twenty switches. Each voltage source is having dc supply of 200V.

4.1. In Phase Disposition Level-Shift PWM Technique (IPDPWM)

The simulink model to generate gate pulses required for inverter using IPDPWM method is shown in Fig.9.

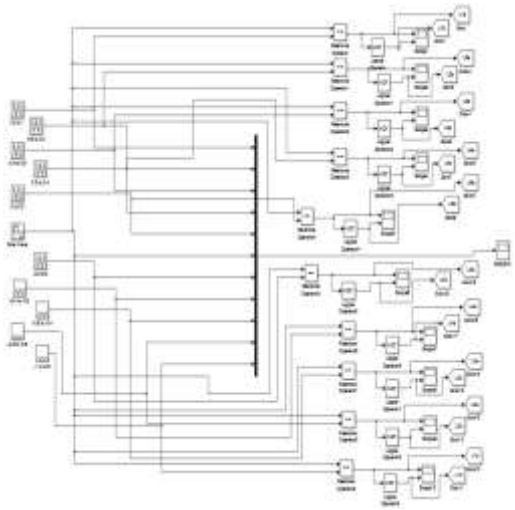

Fig.9: Simulink model to generate gate pulses using IPDPWM technique

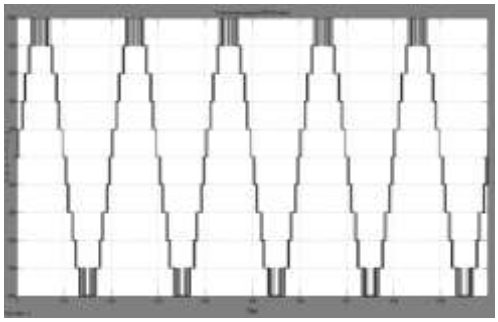

Fig.10: Simulated output voltage waveform of eleven level inverter output IPDPWM technique

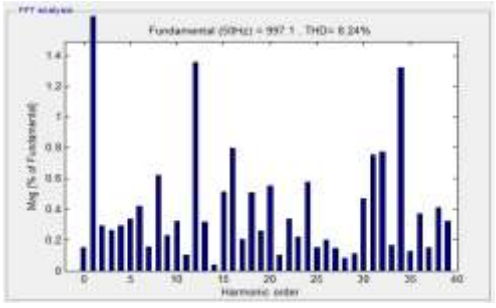

Fig.11: Simulated FFT analysis of inverter output voltage using IPDPWM technique

Using IPDPWM technique we are achieving 8.24% THD.

4.2. Phase Opposition Disposition PWM (PODPWM)

The simulink model to generate gate pulses required for inverter using PODPWM method is shown in Fig.12.

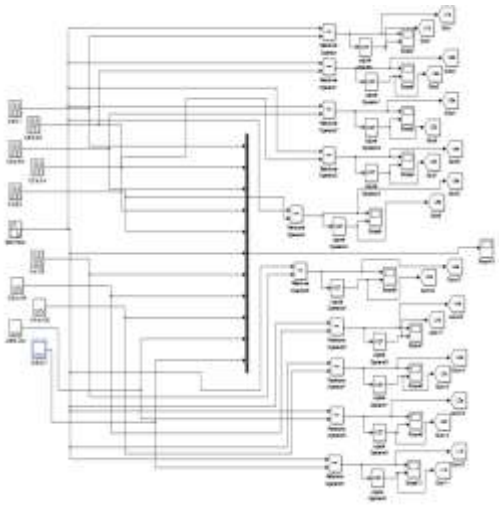

Fig.12: Simulink model to generate gate pulses using PODPWM technique

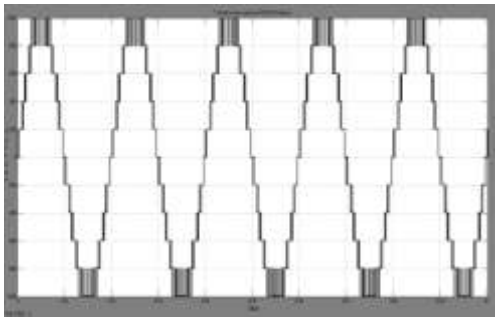

Fig.13: Simulated output voltage waveform of eleven level inverter output PODPWM technique

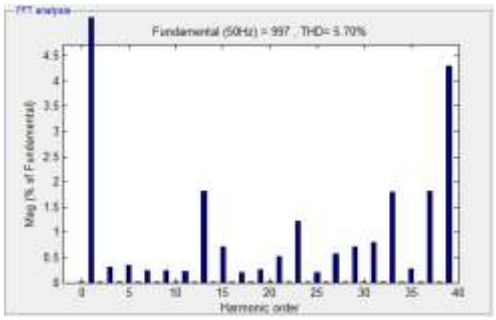

Fig.14: Simulated FFT analysis of inverter output voltage using PODPWM technique

Using PODPWM technique we are achieving 5.70% THD.

4.3. Alternate Phase Opposition Disposition PWM (APODPWM)

The simulink model to generate gate pulses required for inverter using APODPWM method is shown in Fig.15.

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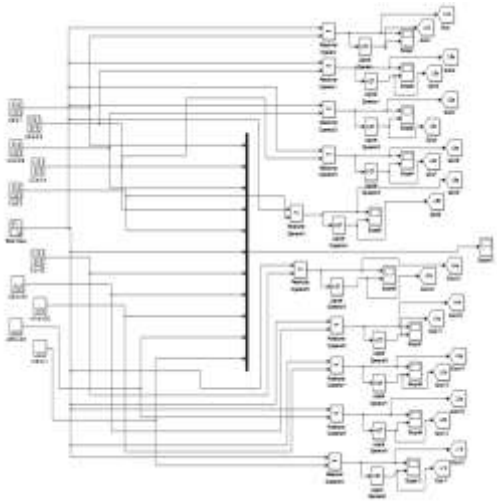

Fig.15: Simulink model to generate gate pulses using APODPWM technique

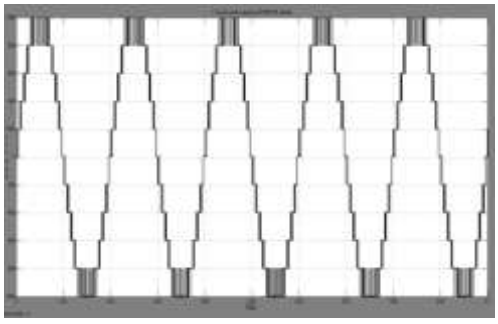

Fig.16: Simulated output voltage waveform of eleven level inverter output APODPWM technique

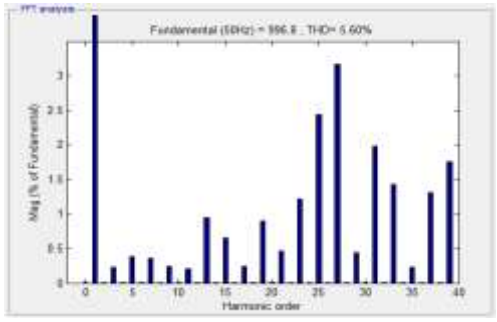

Fig.17: Simulated FFT analysis of inverter output voltage using APODPWM technique

Using APODPWM technique we are achieving 5.60% THD.

4.4. Variable Frequency PWM Technique (VFPWM)

The simulink model to generate gate pulses required for inverter using APODPWM method is shown in Fig.18.

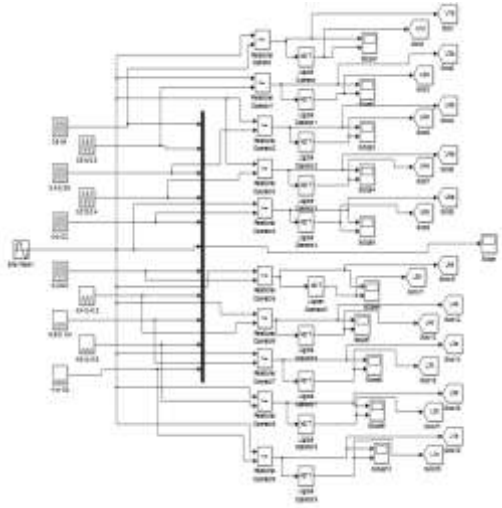

Fig.18: Simulink model to generate gate pulses using VFPWM technique

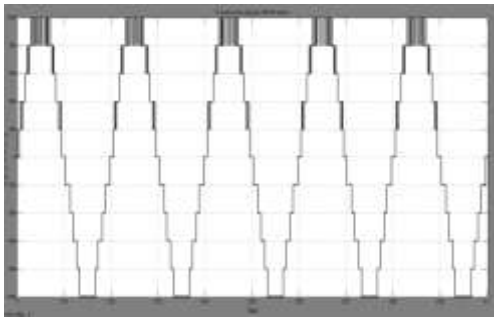

Fig.19: Simulated output voltage waveform of eleven level inverter output VFPWM technique

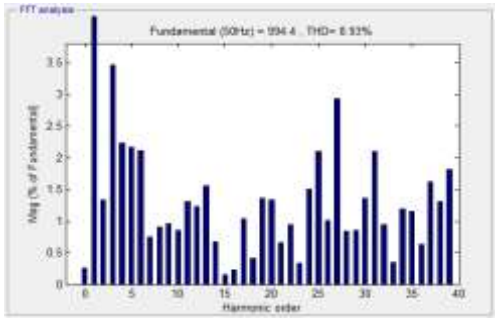

Fig.20: Simulated FFT analysis of inverter output voltage using VFPWM technique

Using VFPWM technique we are achieving 8.93% THD.

Table 2: THD comparisons of different PWM techniques

SLNO	PWM Method	THD%
1	IPDPWM	8.24%
2	PODPWM	5.70%
3	APODPWM	5.60%
4	VFPWM	8.93%

THD comparison of different PWM techniques is shown in Table 2.Based on the THD we can say that which method gives less harmonics is the best PWM method comparing to other three methods. Alternate Phase Opposition Disposition PWM Method is good for this type of inverter.

V. CONCLUSION

Implementation of an eleven level inverter is designed and simulated. Various pulse width modulation techniques are used those are In phase disposition pulse width modulation (IPDPWM), Phase opposition disposition pulse width modulation (PODPWM), Alternate phase opposition disposition pulse width modulation (APODPWM) and Variable pulse width modulation (VFPWM) have been simulated and compared using MATLAB. From the obtained simulation results, it's observed that APODPWM method produces less amount of harmonics compared to other techniques. This PWM technique is the best PWM technique for inverter switching compared to other three techniques. We are obtaining 5.60% total harmonic distortion using APODPWM method.

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