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COMPARISON OF DIFFERENT MULTIPLIERS BASED ON THEIR PERFORMANCE PARAMETERS

Mrs. M. Poornima[1], M. D. Nandhini[2], M. Navaniswar Reddy[3], M. Madhumitha[4], P. Hemasimha[5], P. Venkatesh[6]

[1]*Assistant Professor, Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.*

[23456]*B.Tech Students, Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.*

ABSTRACT

Multiply and Accumulate (MAC) is the basic block that is used in each and every processor which consists of multiplier, adder and accumulator which in turn helps in increasing the speed of the complete processor. Its parameters such as LUT utilization and delay decides the performance of a DSP. So, there is a need to design area and delay efficient multiplier. A comparison is done between Vedic, Wallace, booth on comparing with various parameters like area, delay and speed. The best one is selected as per area, speed and delay constraints and that MAC is considered. The entire design is implemented in Verilog HDL. Synthesis and simulations were done using Xilinx ISE Design Suite 14.5. Here, we achieve significant improvement in area and delay.

Keywords: *MAC, Vedic mathematics, look up table, Xilinx.*

1. INTRODUCTION

In a "Digital Signal Processor" (DSP), the commonly used operations are "multiply and accumulate" (MAC), convolution and "Fast-Fourier Transforms" (FFT) etc. The multiplier is
considered as an essential block for the above operations. Power consumption in a DSP hugely depend on MAC unit. MAC unit consists of a multiplier, an adder for adding its partial products and an accumulator for storing the obtained results. So, for improving the speed of MAC unit, speed of the multiplier should be improved. MAC unit performs both multiply and addition functions. Its parameters such as LUT utilization and delay decides the performance of a DSP. As multiplication is termed as a widely used arithmetic operation, the research has always been aiming to design fast multipliers either by showing improvements in power, area or delay.

2. LITERATURE REVIEW

The Multiplier-accumulator (MAC) unit supports large number of digital signal processing (DSP) applications. Multiply and Accumulator assumes a significant part to choose the presentation of any DSP block. The better presentation of MAC unit satisfies the boundary of quick calculation and continuous handling abilities of a DSP. Multiply and accumulate is a basic block that is used in every processor which consists of multiplier, adder and accumulator. MAC unit performs both multiply and addition functions its parameters such as delay and area. In this paper, Vedic and Booth multipliers are the existing methods. To enhance the performance of the processor it is required to design a high speed, area and delay efficient multiplier i.e., Wallace multiplier. Referenced design is executed in Verilog HDL.

3. EXISTING METHOD

Most of the DSP processors has MAC as its basic functional unit which performs complex multiplication and addition operations. Vedic multiplier and Booth multiplier has less delay and area. In a MAC unit multiplier are the essential block that determine the combinational path delay and area required to implement the hardware, so in this we need to design a high speed and area optimized multiplier i.e., Wallace multiplier.

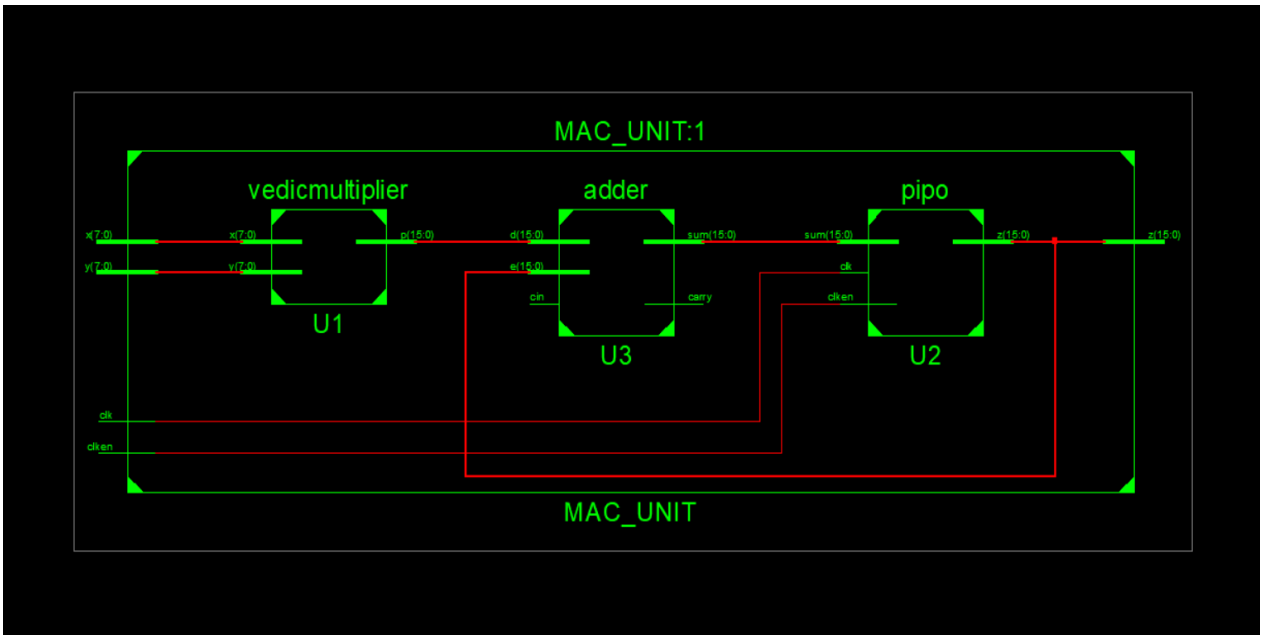

Figure 1: RTL Schematic for Vedic Multiplier based MAC

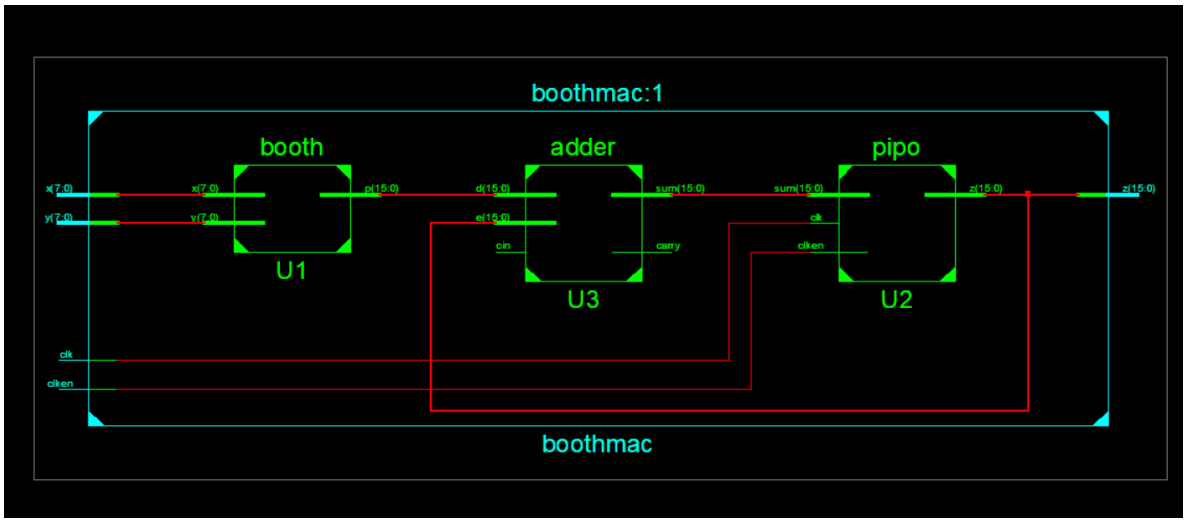

Figure 2: RTL Schematic for Booth Multiplier based MAC

4. PROPOSED METHOD

A comparison is done between Vedic, Booth, Wallace MAC's on comparing with various parameters like area, delay and speed. The best one is selected as per area, speed and delay constraints considered. The Synthesis and simulations were done using Xilinx ISE Design Suite 14.5.

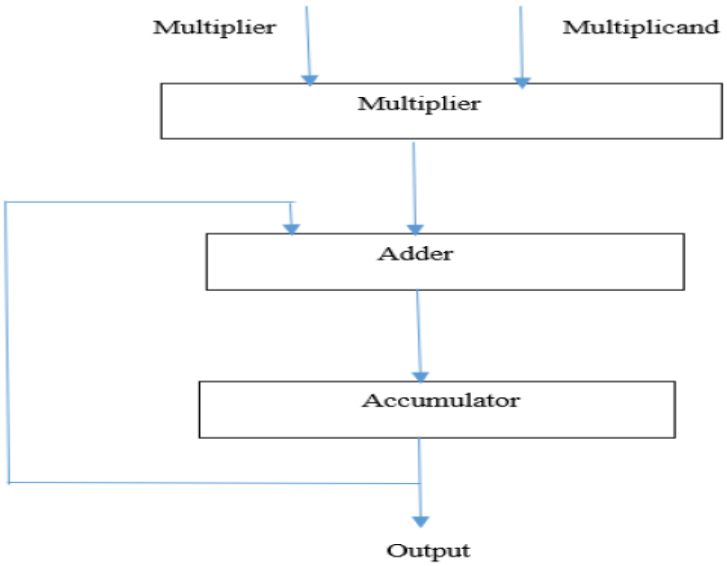

Figure 3: Block diagram of MAC

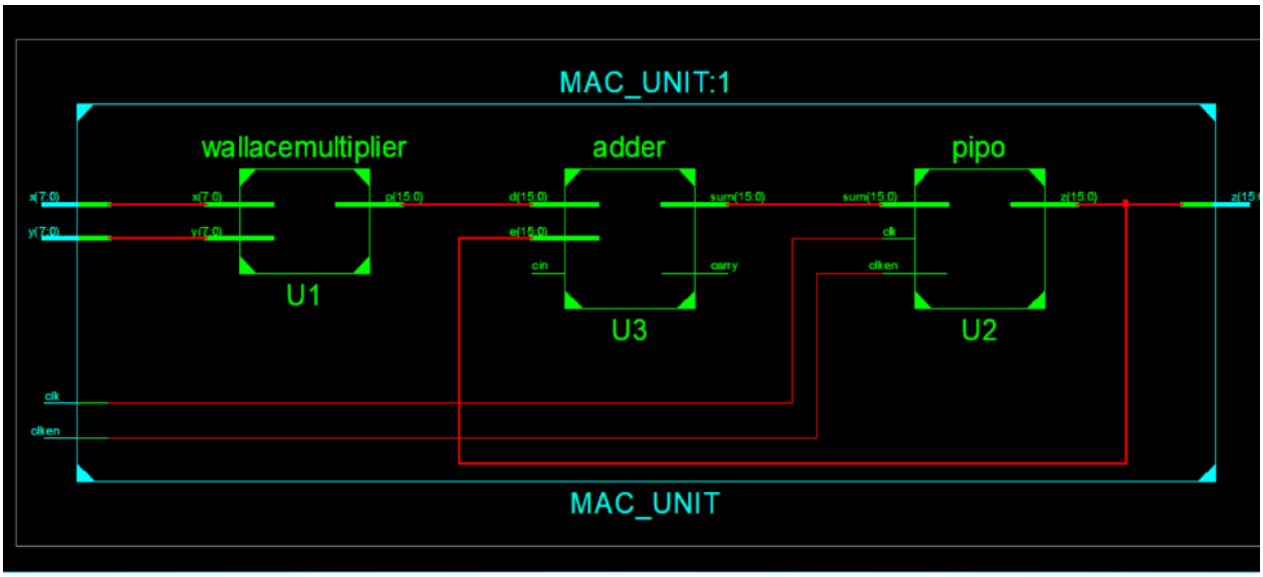

Figure 4: RTL Schematic for Wallace Multiplier based MAC

5. METHODS OR TECHNIQUES USED

The proposed Wallace multiplier is implemented in Verilog HDL stimulated in Xilinx ISE Design Suite 14.5. Verilog HDL is a hardware description language. It is a language used for describing a digital system like network system. It is very easy for designing and debugging.

6. SIMULATION RESULT

From the analysis of all multipliers, wallace multiplier is the best multiplier. It has less area and less delay when compared to vedic and booth multipliers. This comparison helps us to select a suitable multiplier for a particular task or application.

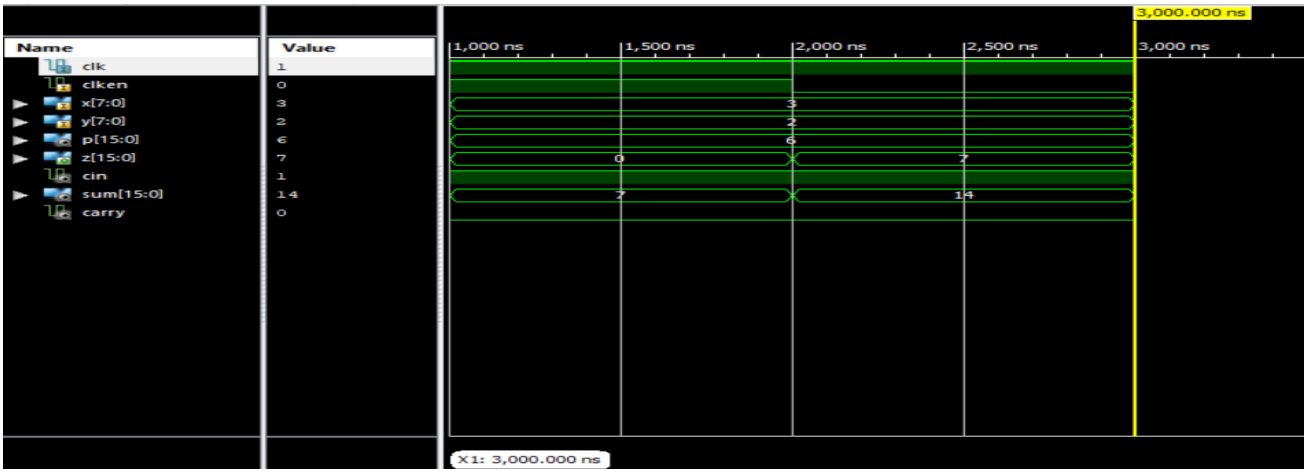

Figure 5: Simulation result for Wallace Multiplier Based MAC

Multiplier Type	Delay	No of Slice LUT's Used (Area)	%LUT utilization
Vedic	27.162ns	184 out of 63400	0%
Booth	26.535ns	150 out of 20400	0%
Wallace	26.222ns	75 out of 20400	0%

Table 1: Comparison of implemented Multipliers

7. CONCLUSION

In this paper, three multipliers are compared with each other on basis of delay, area and speed. By comparing both existing and proposed multiplier, it is concluded that Wallace Multiplier has less delay and area when compared with the Vedic and booth Multiplier. In the existing system, the Vedic multiplier has a delay of 27.162ns and Booth multiplier has 26.535ns. In the proposed system, the Wallace multiplier has 26.222ns. On the study of above comparison, Wallace Multiplier has high speed and having lot of advantages.

8. FUTURE SCOPE

For future research, a better multiplier can be proposed by modifying these multipliers and a better comparison of various multipliers with the proposed modified multiplier can be done by taking all multipliers simultaneously in one table. That will give more accurate comparison in percentage values.

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