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DESIGN OF QPSK MODULATOR FOR WI-FI AND DSP APPLICATIONS

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ABSTRACT

This thesis signifies the propose technique of modulator for Quadrature phase shift keying (QPSK). QPSK is one kind of phase shift keying which is under the digital modulation. The digital modulation is extra capable in long distance transmission and extra protected evaluated to other. The noise identification and accusation are better in digital techniques over analog techniques. Convert the input information in digital and transfer over analog channel is defined the digital modulation. In these days, main factor to be believed is low power and less time. Shift keying methods describes as the carrier bit stream modifies in single or extra parameters supported on the input bit stream, which we require to transmit. This present method is intended in Verilog HDL as well as synthesized on XILINX ISE tool.

***Keywords*— QAM, ASK, BPSK.**

I. INTRODUCTION

Digital techniques have replaced analog techniques in present growing world. Modulation is the process of diverging the carrier signal. Digital modulation is described as the developing of digital data broadcast from transmitter to receiver over the analog informational channel (medium). In this process of modulation, the excite wave changes the constraints of carrier wave. Usually we consider that amplitude, frequency and phase are the parameters for any signal or sequence. The digital modulation is classified depend on the foundation of parameters of carrier wave. In digital modulation, three different techniques have present. These are:

1. Amplitude shift keying
2. Frequency shift keying
3. Phase shift keying.

In digital method, varying in the phase of the carrier is described as Phase Shift Keying. The digital modulators are involved to produce these waves supported on the method we necessitate. QPSK law is regularly exploited in phase shift keying modulators. Both the accuracy and the stability of the generated signals must generally be addressed in the main factors of accuracy and stability. In real time, these are particularly when the constraints of interest have to be modified.

This digital transmission system has confirmed that it is extra capable than analog transmission since the improvements in the fields of Digital Signal Processing (DSP) and Very Large Scale Integration (VLSI). In

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digital broadcast, noise exemption, combining unusual varieties of message, protection has progressed and benefit above analog broadcast. Phase shift keying utilizes a finite number of phases not like all extra digital modulation methods, which exploits finite number of discrete signals to characterize the data.

II. LITERATURE SURVEY

1.1 Quadrature Amplitude Modulation

For speedy digital signals, the main modulation method is this QAM. This QAM develops into our daily handling system as wireless protocols, modems to military for personal communications. In QAM, the two carriers are of 90 degrees outside phase and makes change in the amplitude of the carrier waves.

Performance of QAM has done in three stages i.e., modulation, transmission and demodulation. In this article, we are focusing on modulation itself. The modulation entails two stages:

1. Serial to parallel conversion
2. Digital to analog conversion

In serial to parallel conversion, it changes the bit flow into log2*M* streams, where *M* is number of symbols. The bit rate is described as 1/log 2*M*.

In second digital to analog conversion, the input streams have index a look up table. Single signal transforms quadrature Q, carrier and the extra modulates in-phase I, carrier. Sampling rate of the method is larger than the symbol rate then it is known as analog. Here we can't fine true analog system. At last append Q and I wave to outline a QAM signal.

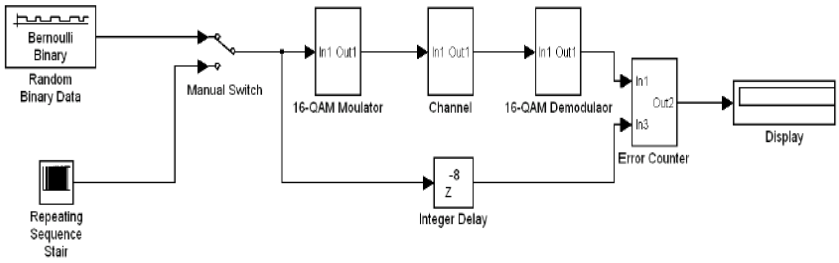

Fig 1: Example diagram for 16-QAM

1.2 Binary Phase Shift Keying

BPSK also known as phase reversal keying (PRK) or two phase shift keying. This is easiest form of PSK. It gets two phases parted by 180 degrees. That's the reason why generally it is acknowledged as 2-PSK. We can't say where these points have located. It has many disadvantages like the highest rate of noise distortion, would proficient to transmit 1 bit/symbol. So, this is not appropriate for high data transmission applications.

In BPSK, the term "binary" is indicating that it can transfer one binary valued quantity within bit duration. Phase shifting made by π. Keying returns to the first electrical communication system. This is a technique of transferring the data on carrier. That carrier wave would be base band signals or free- space transmissions otherwise large context of another signal. This provides carrier, for which phase is changes between 0 and 180 degrees. BPSK is admired in logical design and since the immunity of noise makes demand in many fields.

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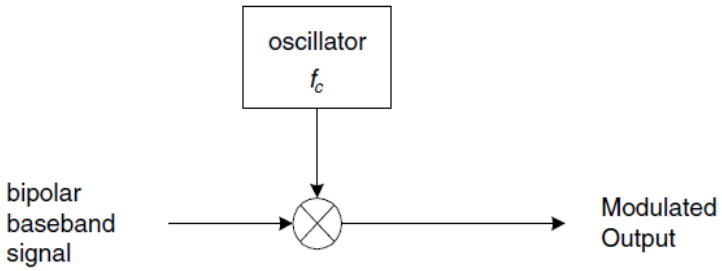

Fig 2: BPSK modulator

The above figure illustrates the BPSK modulator. The response of the modulator is defined as

$$X(t) = I(t) + jQ(t).$$

III. PROPOSED METHOD

3.1 Quadrature phase shift keying (QPSK):

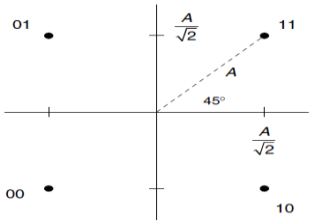

Fig 3: Ideal QPSK constellation

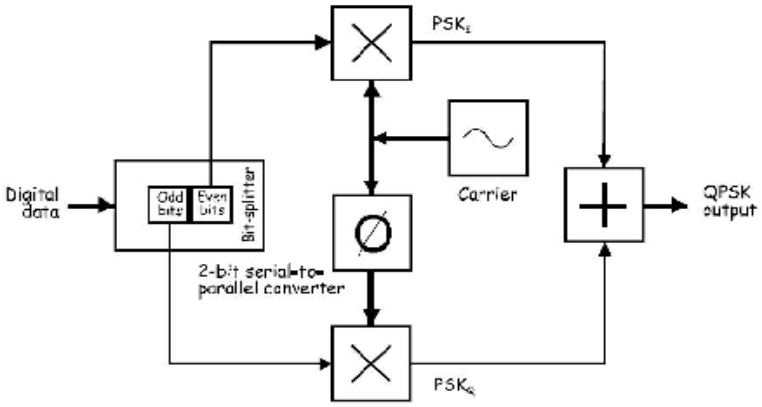

Fig 4: Block diagram of QPSK

QPSK is solitary of the kinds of phase shift keying. This is related with the BPSK. This scheme also uses double side band carrier suppression scheme as similar to BPSK however the diversity is it would proficient to launch two bits of digital flow concurrently. This makes more amount of users would proficient to access on the channel.

The generation of QPSK is exhibited in fig 4. The excite data is straight provided to the bit splitter to split it as even (i.e., 0, 2, 4....) and odd (1, 3, 5.....) bits. These even bits are straight multiplied with the carrier wave in the multiplier block to produce BPSK signal i.e., PSK_I as illustrated in figure. At the similar time remaining odd bits are multiplied by the 90 degrees phase shifted carrier signal in the other multiplier block to produce another

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BPSK signal i.e., PSK_Q. Afterward the both BPSK signal basically appended in adder obstruct and sends to output.

This architecture has used the trigonometric characteristics as defined as below

$$I \cos \omega ct + Q \sin \omega ct = R \cos (\omega ct + \theta)$$

Where $R = \sqrt{(I^2 + Q^2)}$ and

$\theta = \tan^{-1}(Q/I)$.

The transformed signal is described as simple as

$X(t) = I(t) + Q(t)$.

There the complex signal X(t) is outlined by using in-phase component as real part and Quadrature component as imaginary part. Currently we are going to discuss about constellation part.

Constellation:

There are four possibilities for transmission i.e., 00, 01, 10 and 11. At every possibility the modulator shifts the phase of carrier wave i.e., $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ as exhibited in fig 3. Each output differs by one bit only. Hence, it is acknowledged as 4 PSK. QPSK has to keep the information rate either double of BPSK data rate while keep the bandwidth of the signal or at the time of half bandwidth needed, this utilizes same information rate of BPSK. QPSK outcomes in two performances; these are in-phase element and Quadrature element of the signal.

3.2 Flow chart for QPSK process:

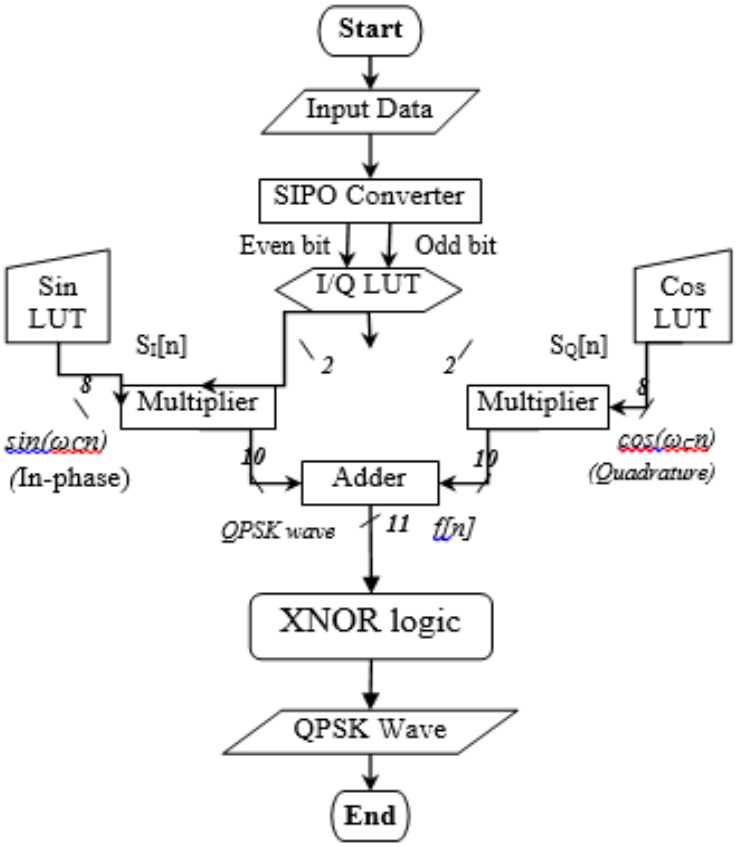

Fig 5: Flow chart of QPSK

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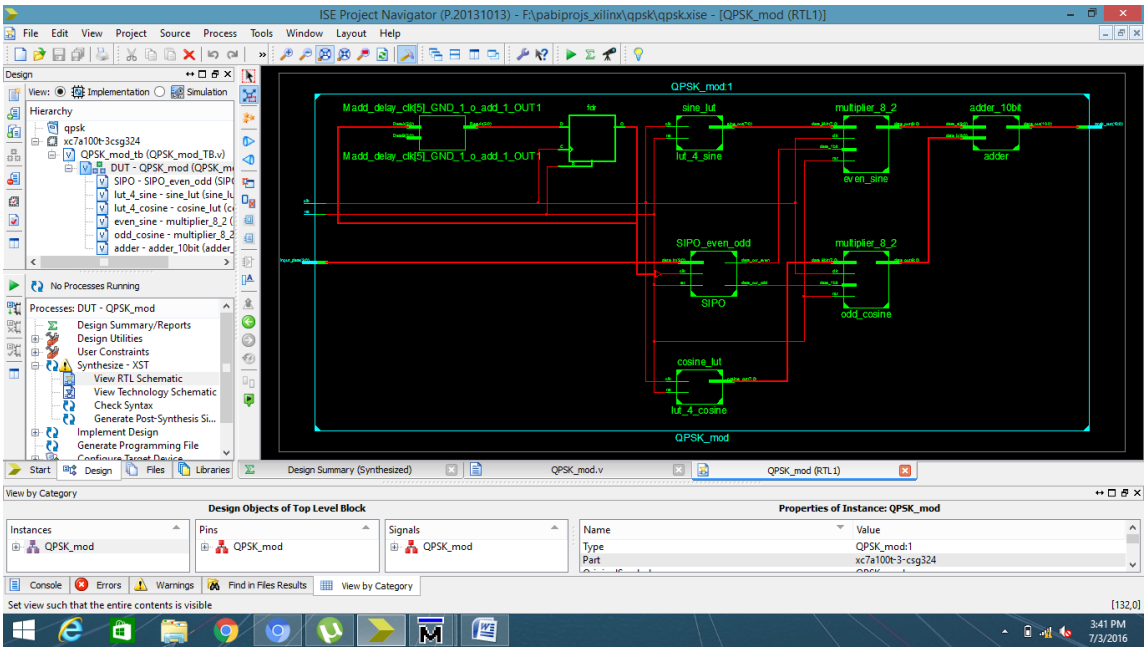
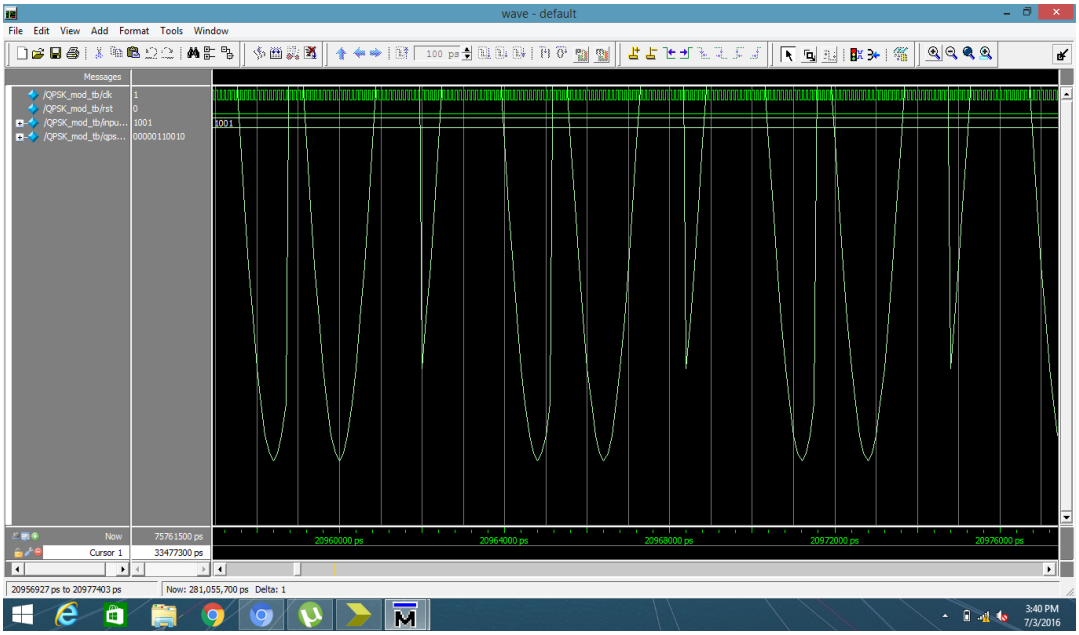
We can examine that the excite data honestly specified to the SIPO converter from the beyond flow chart. It separates the excite information as even and odd. These even and odd are produced in split multipliers by sinusoidal and cosine signals correspondingly. Here the sinusoidal signal is in phase component and the cosine wave is quadrature phase element. The outputs of both the multipliers are adder in adder block. It presents the response acknowledged as QAM. This wave is promoted during a XNOR logic gate to get QPSK w i.e., output. Simulation outcomes as well as conclusion have shown in below discussions.

IV. SIMULATION RESULTS

In this thesis we have been designing the QPSK using the Verilog HDL as well as synthesised in MODEL SIM6.2. This synthesis reports yielding that expected wave forms are matching with the practical results shown here.





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V. CONCLUSION

The architecture of QPSK has designed and verified. It would proficient two transport two bits per symbol using four phases leads to minimize the chip area and decreases the power consumption. Our structure minimizes the amount of blocks to perform this technique. The obtained simulation results are verified successfully.

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